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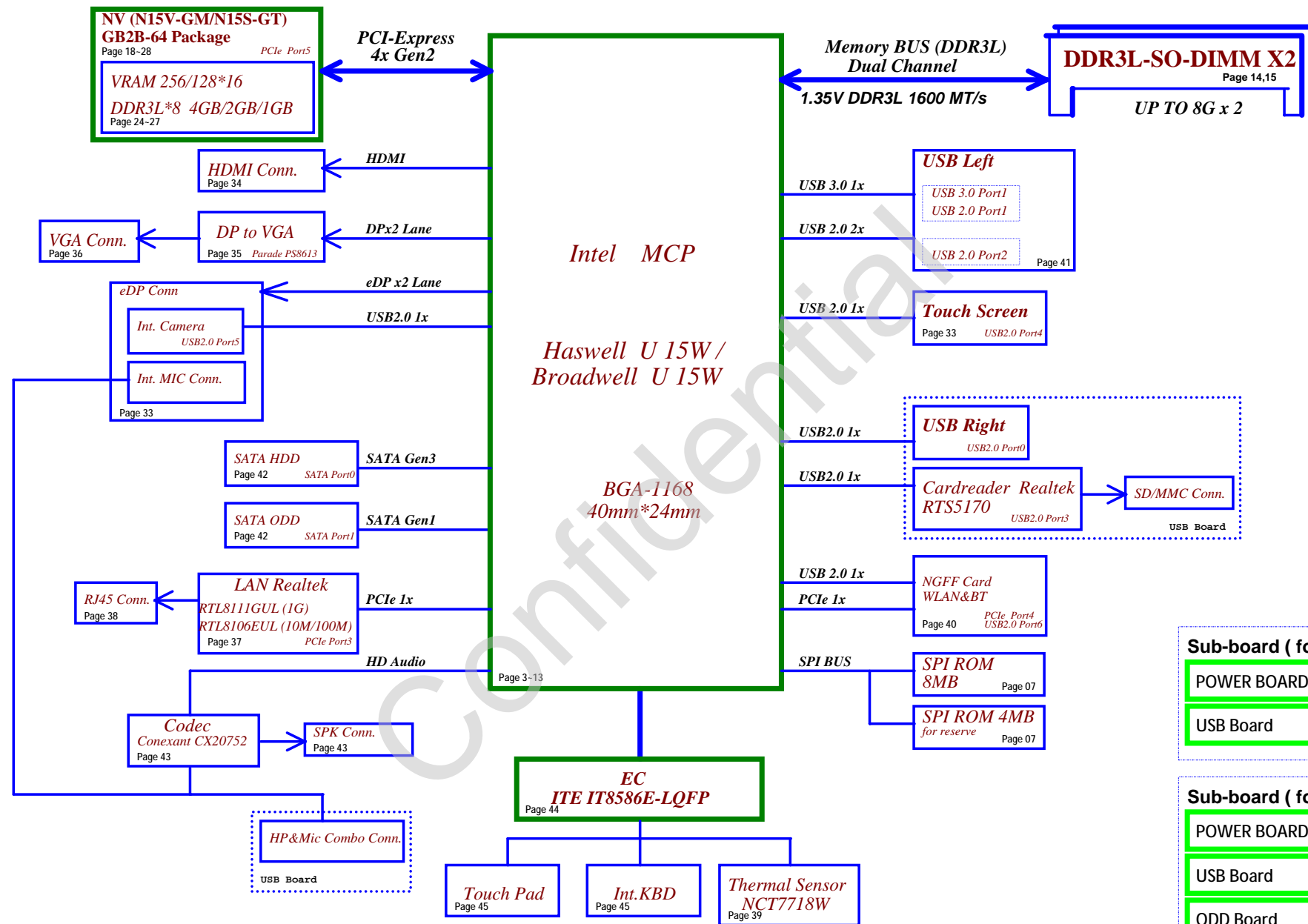
ACLUA M/B Schematics Document

Intel Haswell/Broadwell U-Processor with DDRIII L + NV (N15V-GM/N15S-GT) GPU

2013-12-26

REV: 0.3

Security Classification	LC Future Center Secret Data			Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Cover Page	
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Title		Block Diagram	
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Voltage Rails (0 --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+3VALW_PCH	+1.35V	+5VS +3VS +1.5VS +1.35VS +1.05VS +0.675VS CPU_CORE +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VAL#	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0 EHCI1		USB 3.0 XHCI	
0	USB Port (Right Side)		
1	USB Port1 (Left Side)	1	USB Port1 (Left Side)
2	USB Port2 (Left Side)	2	
3	Cardreader	3	
4	TOUCH PANEL	4	
5	Camera		
6	NGFF(WLAN)		
7			

BOM Structure Table

[illegible]

SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	V +3VALW_PCH	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

PCIE PORT LIST

Port	Device
1	
2	
3	LAN
4	WLAN
5	Discrete GPU
6	

EC SM Bus1 address

EC SM Bus2 address

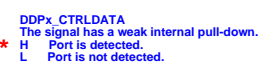
PCH SM Bus address

EC SW Bus1 address		EC SW Bus2 address	
Device		Device	Address
Smart Battery	0X16	Thermal Sensor NCT7718W	1001_100xb
Charger	0001 0010 b	VGA	0x41(default)
		PCH	need to update

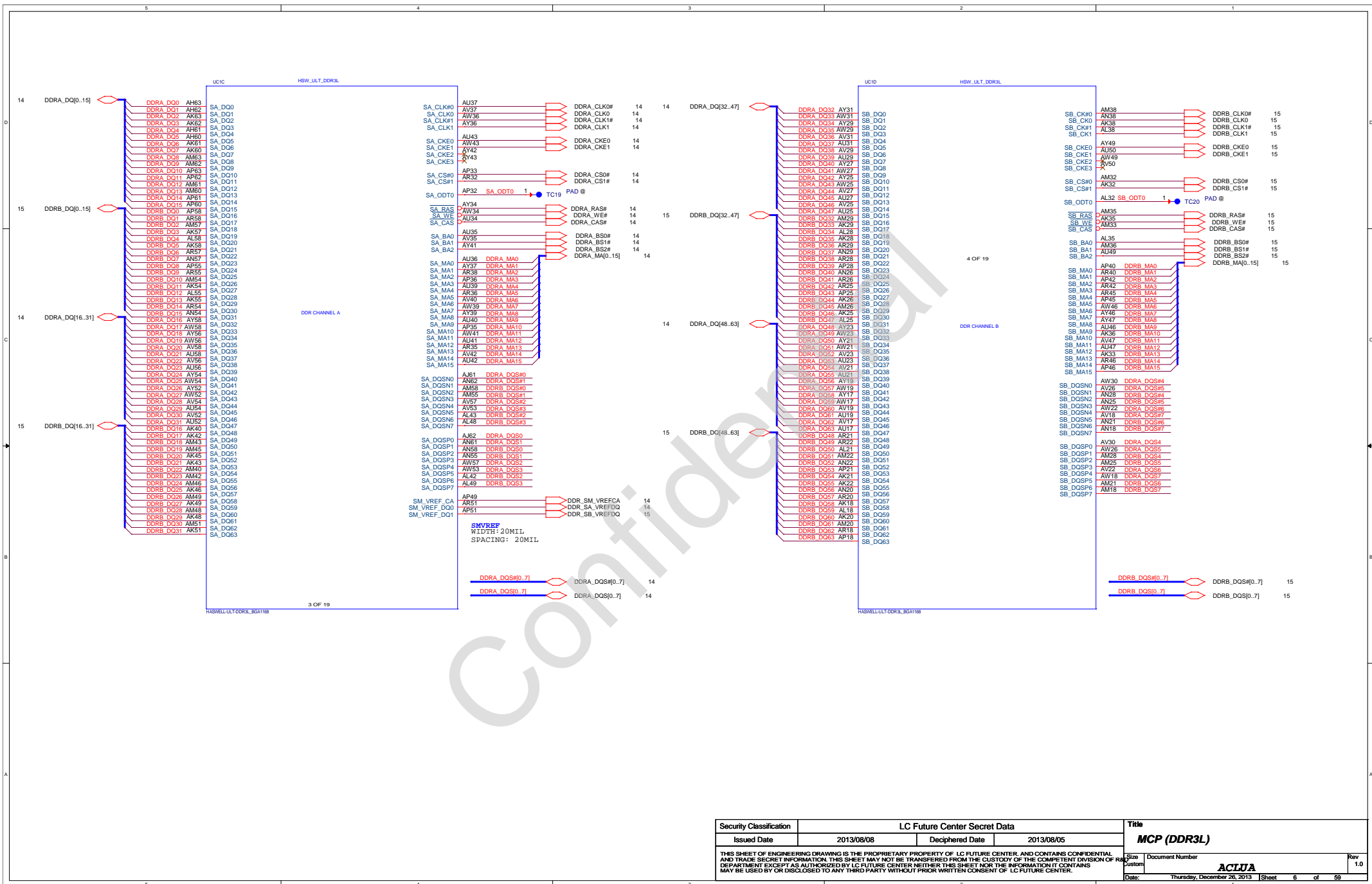
Device	Address
DDR DIMMA	1010 000Xb
DDR DIMMB	1010 010Xb
Wlan	Rsvd

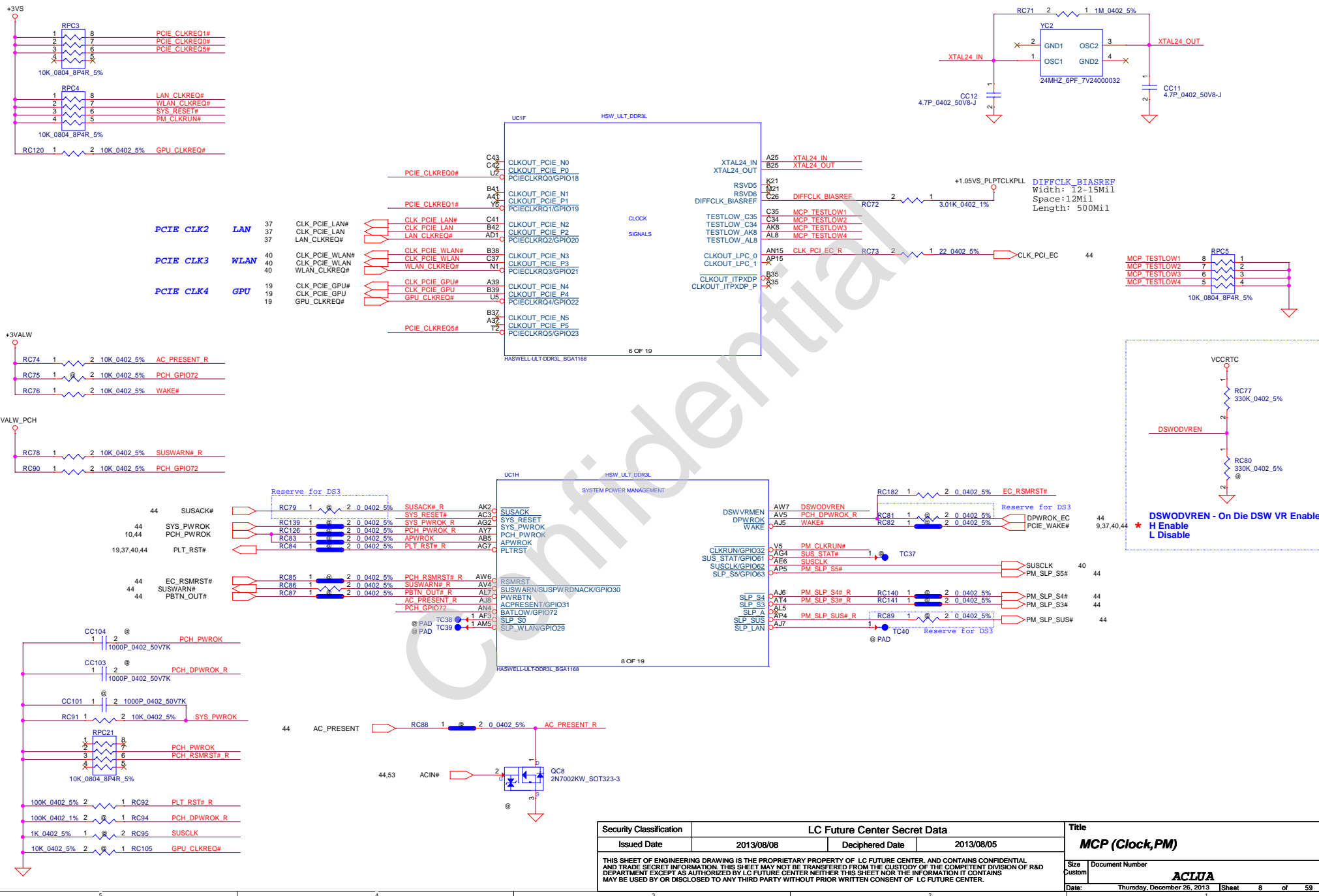
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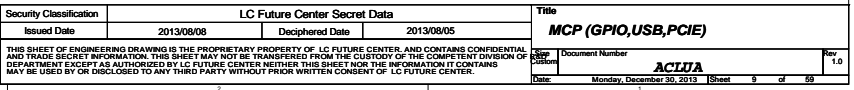
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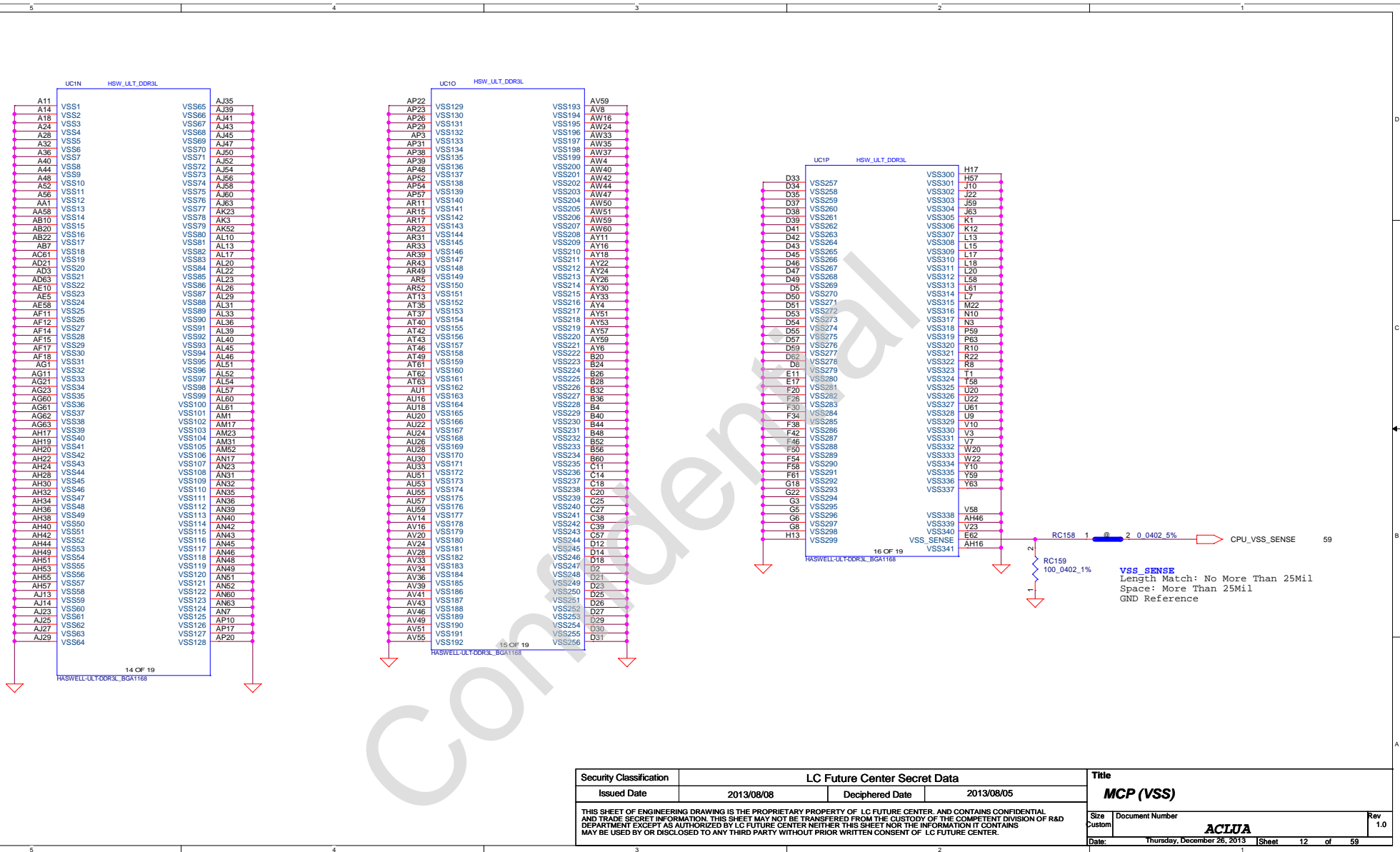








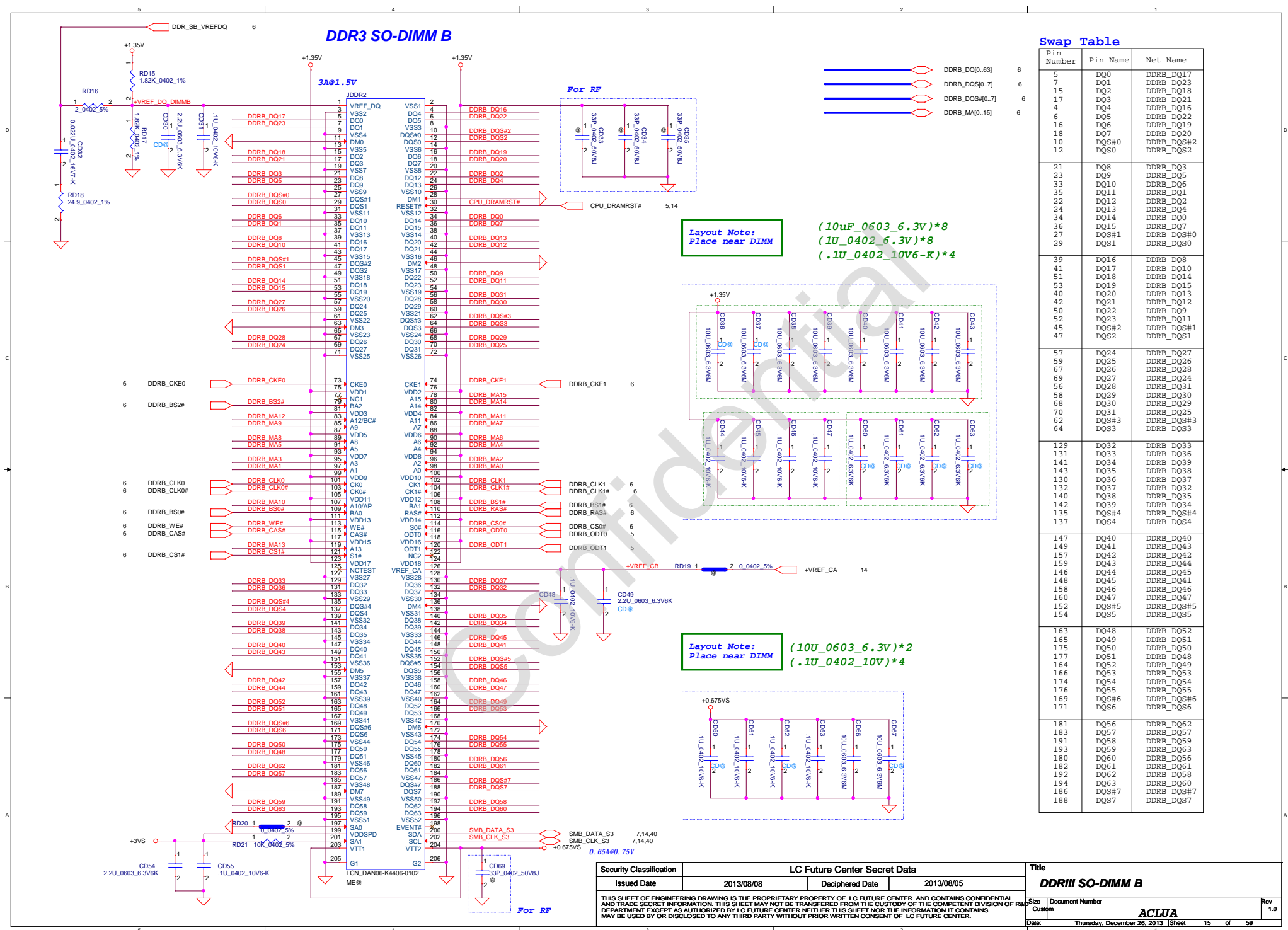
	Title
	<i>MCP (Power)</i>



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Pin Number	Pin Name	Net Name
5	DQ0	DDR0_DQ17
7	DQ1	DDR0_DQ23
15	DQ2	DDR0_DQ18
17	DQ3	DDR0_DQ21
4	DQ4	DDR0_DQ16
6	DQ5	DDR0_DQ22
16	DQ6	DDR0_DQ19
18	DQ7	DDR0_DQ20
10	DQS#0	DDR0_DQS#2
12	DQS0	DDR0_DQS2
21	DQ8	DDR0_DQ3
23	DQ9	DDR0_DQ5
33	DQ10	DDR0_DQ6
35	DQ11	DDR0_DQ1
22	DQ12	DDR0_DQ2
24	DQ13	DDR0_DQ4
34	DQ14	DDR0_DQ0
36	DQ15	DDR0_DQ7
27	DQS#1	DDR0_DQS#0
29	DQS1	DDR0_DQS0
39	DQ16	DDR0_DQ8
41	DQ17	DDR0_DQ10
51	DQ18	DDR0_DQ14
53	DQ19	DDR0_DQ15
40	DQ20	DDR0_DQ13
42	DQ21	DDR0_DQ12
43	DQ22	DDR0_DQ9
52	DQ23	DDR0_DQ11
45	DQS#2	DDR0_DQS#1
47	DQS2	DDR0_DQS1
57	DQ24	DDR0_DQ27
59	DQ25	DDR0_DQ26
67	DQ26	DDR0_DQ28
69	DQ27	DDR0_DQ24
56	DQ28	DDR0_DQ31
58	DQ29	DDR0_DQ30
68	DQ30	DDR0_DQ29
70	DQ31	DDR0_DQ25
62	DQS#3	DDR0_DQS#3
64	DQS3	DDR0_DQS3
129	DQ32	DDR0_DQ33
131	DQ33	DDR0_DQ36
141	DQ34	DDR0_DQ39
143	DQ35	DDR0_DQ38
130	DQ36	DDR0_DQ37
132	DQ37	DDR0_DQ32
140	DQ38	DDR0_DQ35
142	DQ39	DDR0_DQ34
155	DQS#4	DDR0_DQS#4
137	DQS4	DDR0_DQS4
147	DQ40	DDR0_DQ40
149	DQ41	DDR0_DQ43
157	DQ42	DDR0_DQ42
159	DQ43	DDR0_DQ44
146	DQ44	DDR0_DQ45
148	DQ45	DDR0_DQ41
158	DQ46	DDR0_DQ46
160	DQ47	DDR0_DQ47
152	DQS#5	DDR0_DQS#5
154	DQS5	DDR0_DQS5
163	DQ48	DDR0_DQ52
175	DQ49	DDR0_DQ51
165	DQ50	DDR0_DQ50
177	DQ51	DDR0_DQ48
164	DQ52	DDR0_DQ49
166	DQ53	DDR0_DQ53
174	DQ54	DDR0_DQ54
176	DQ55	DDR0_DQ55
169	DQS#6	DDR0_DQS#6
171	DQS6	DDR0_DQS6
181	DQ56	DDR0_DQ62
183	DQ57	DDR0_DQ57
191	DQ58	DDR0_DQ59
183	DQ59	DDR0_DQ63
180	DQ60	DDR0_DQ56
182	DQ61	DDR0_DQ61
192	DQ62	DDR0_DQ58
194	DQ63	DDR0_DQ60
186	DQS#7	DDR0_DQS#7
188	DQS7	DDR0_DQS7

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N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

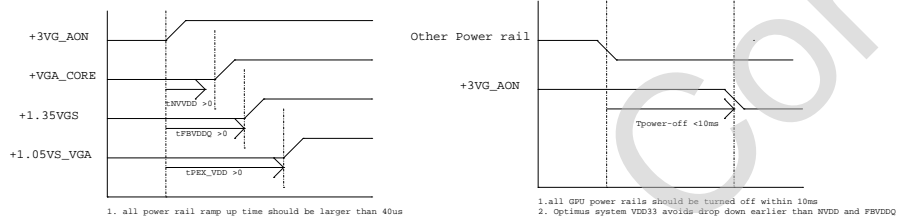
Products	GPU (4) (W)	Mem (1.5) (W)	NVCLK /MCLK (MHz)	NVVDD (V) (A) (W)			FBVDD (1.35V) (A) (W)		FBVDDQ (GPU+Mem) (1.35V) (A) (W)		PCI Express (1.05V) (6) (mA) (W)		I/O and PLLVDD (1.05V) (mA) (W)		Other (3.3V) (mA) (W)	
N14X 128bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

N15x Multi-level Straps

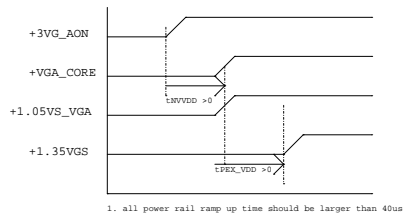
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

N15V-GM Power Sequence



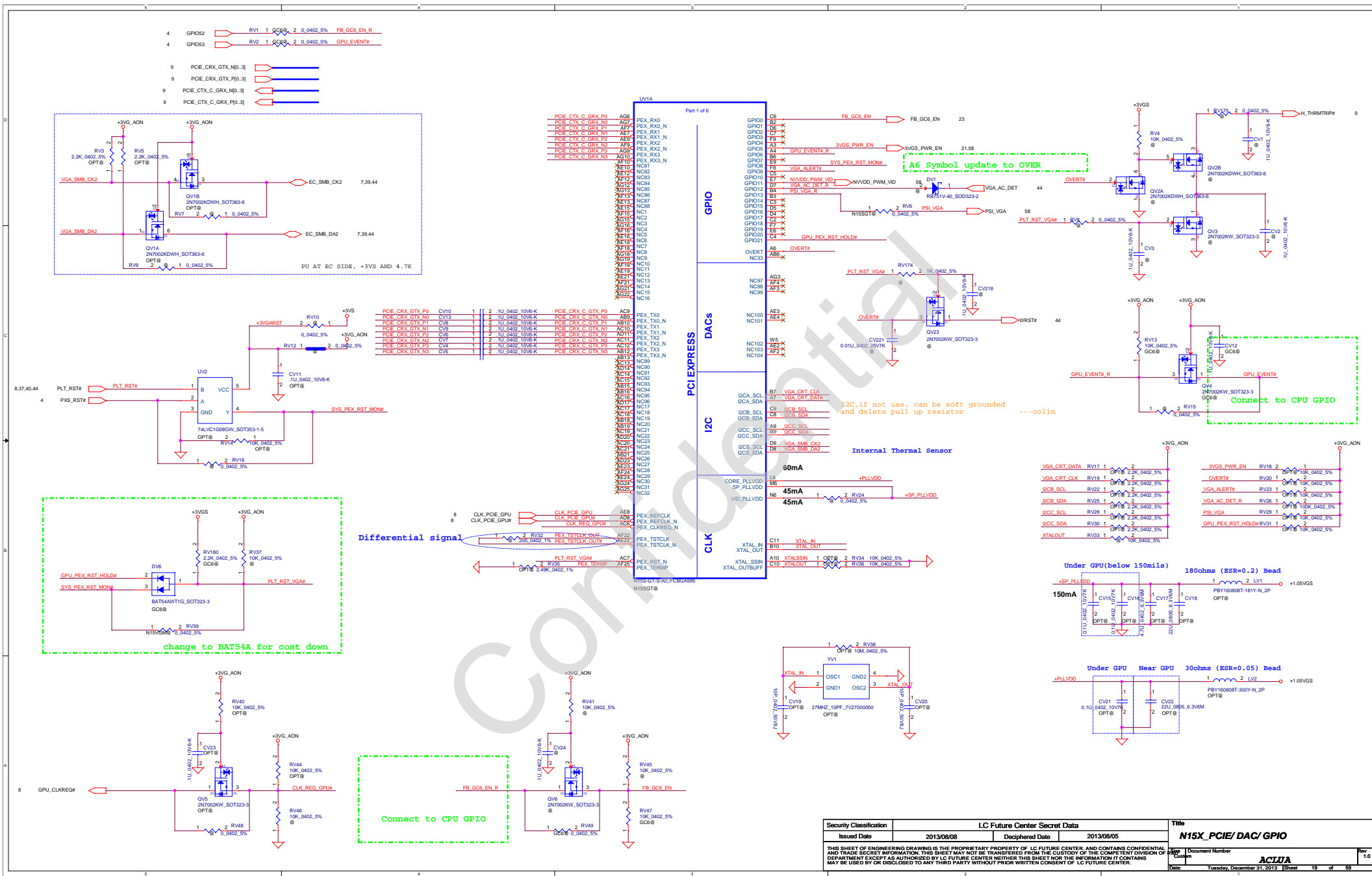
N15S-GT Power Sequence



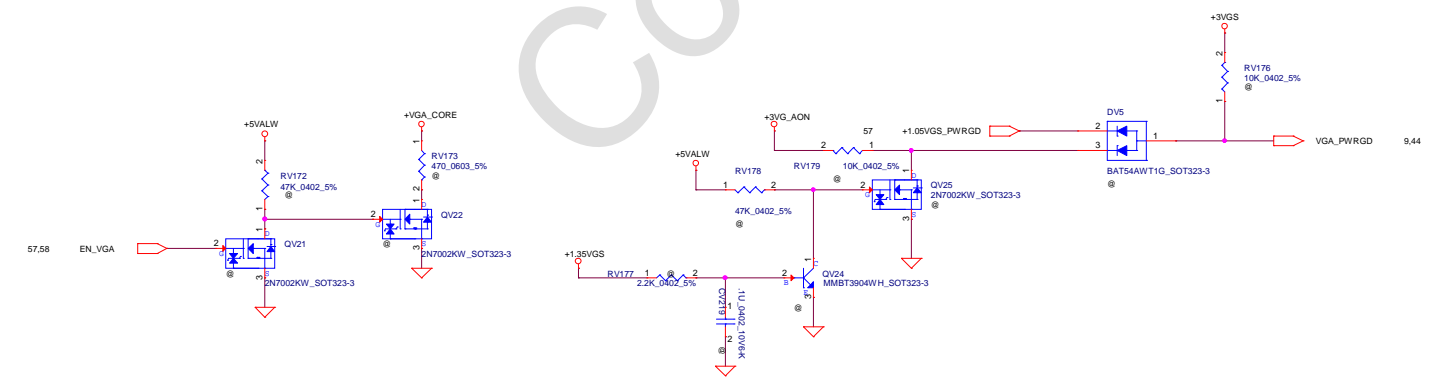
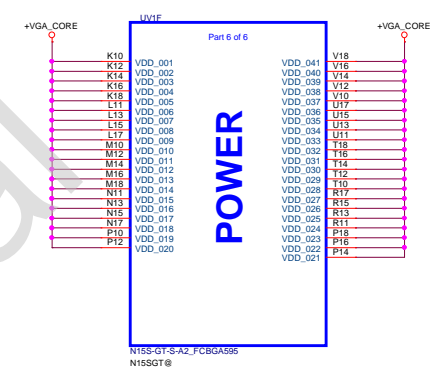
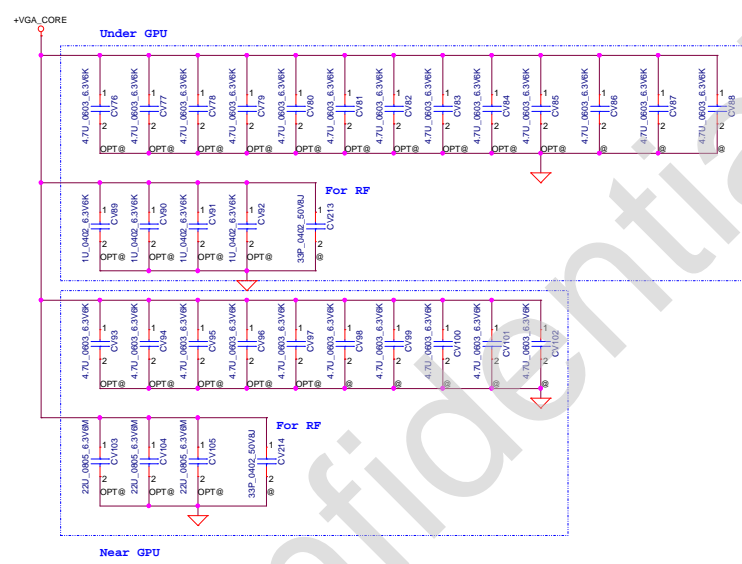
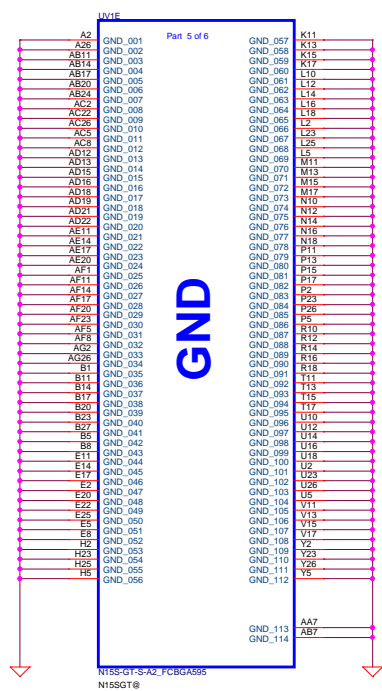
N15x Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

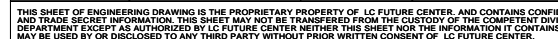
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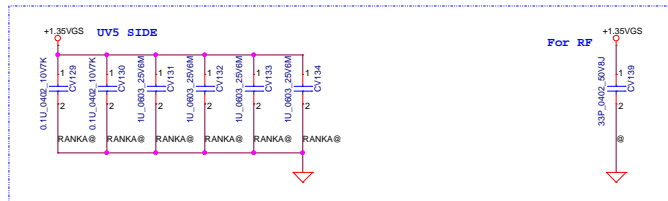
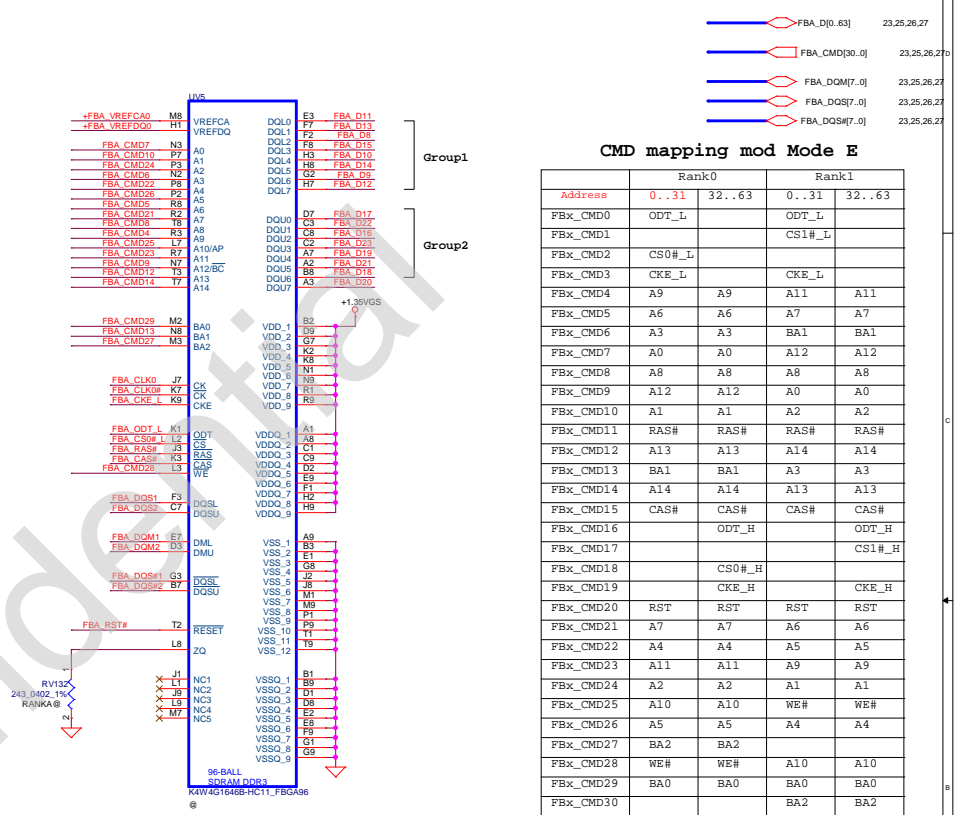
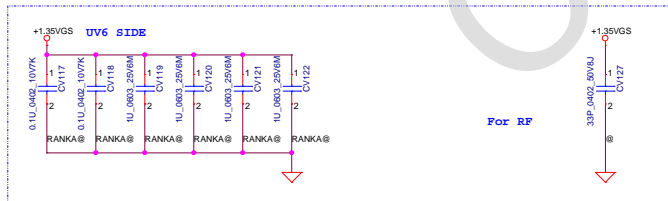
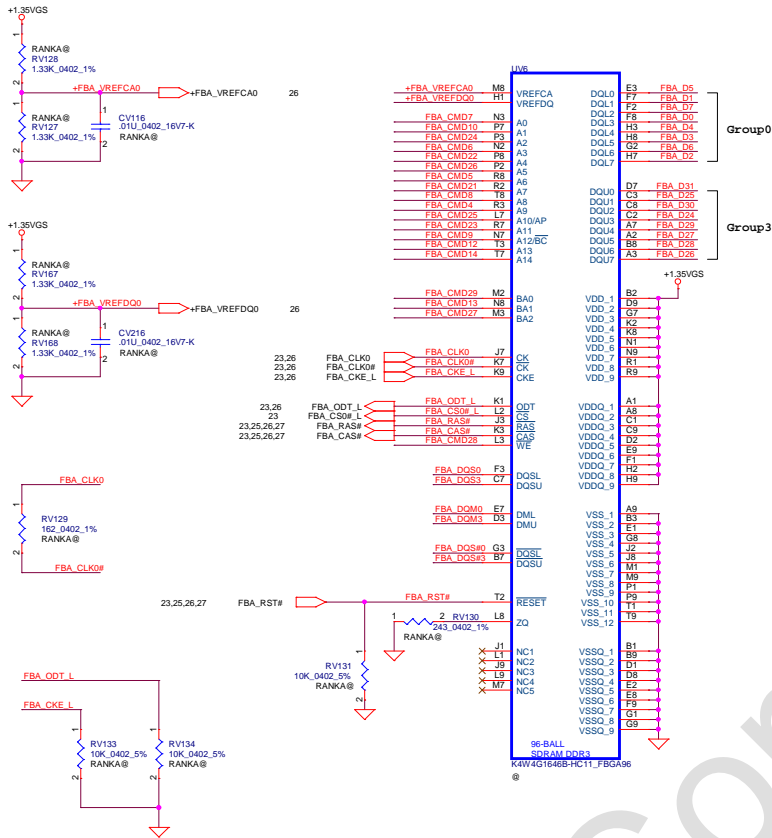
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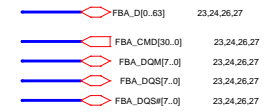
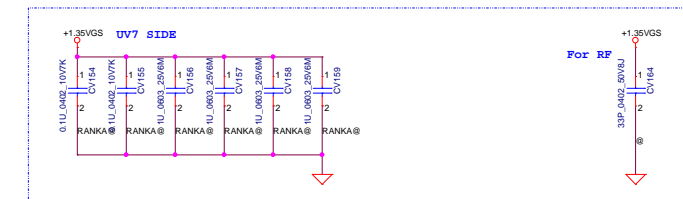
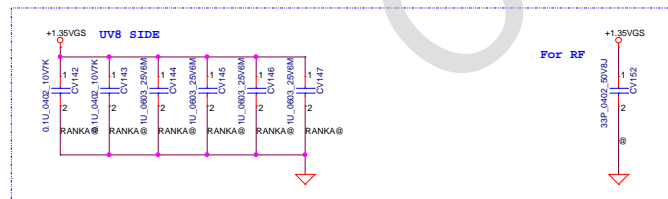
at least 16 mils width(optimal)
20 mils spacing to other signals /planes



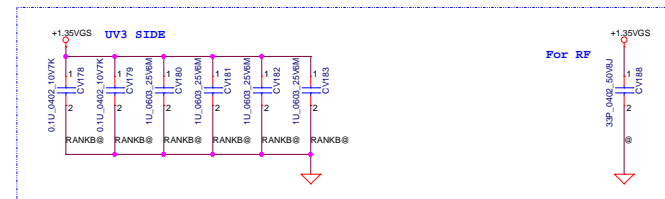
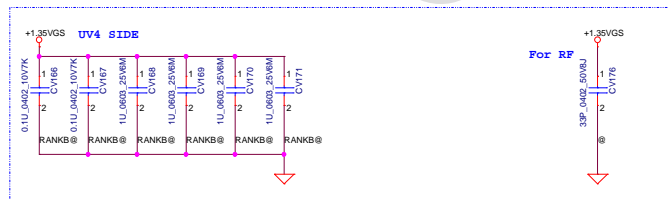
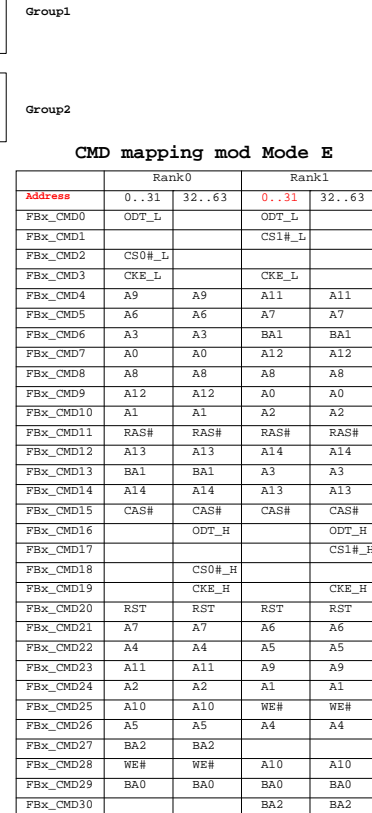
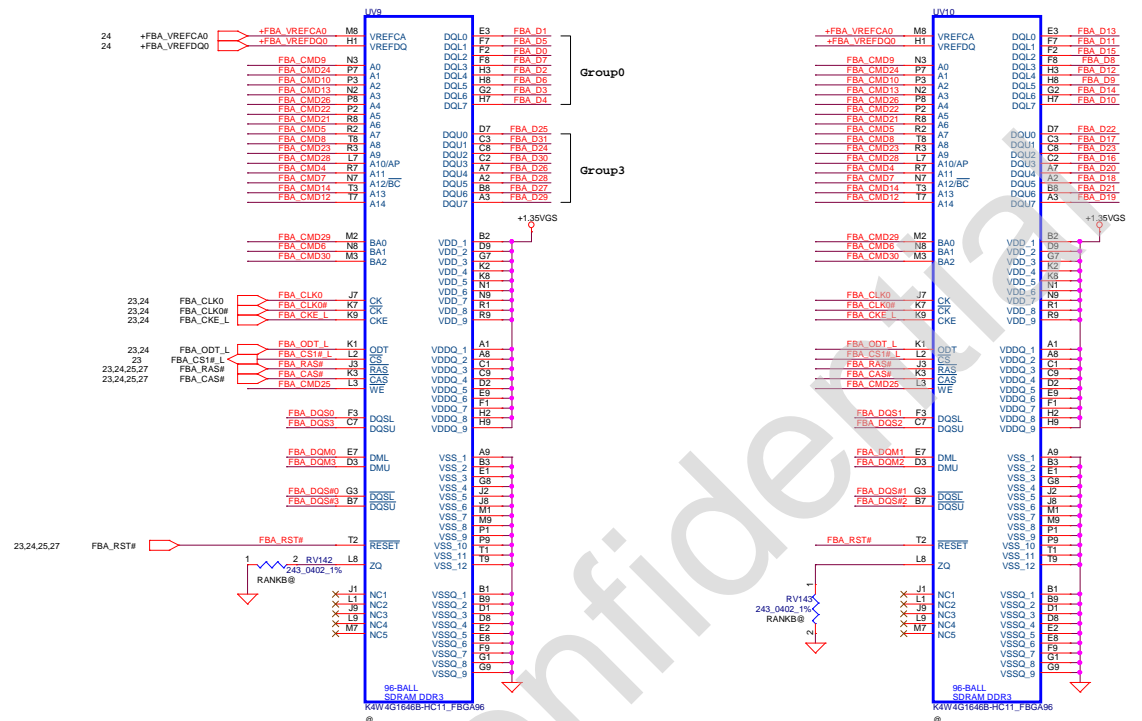
CMD mapping mod Mode E

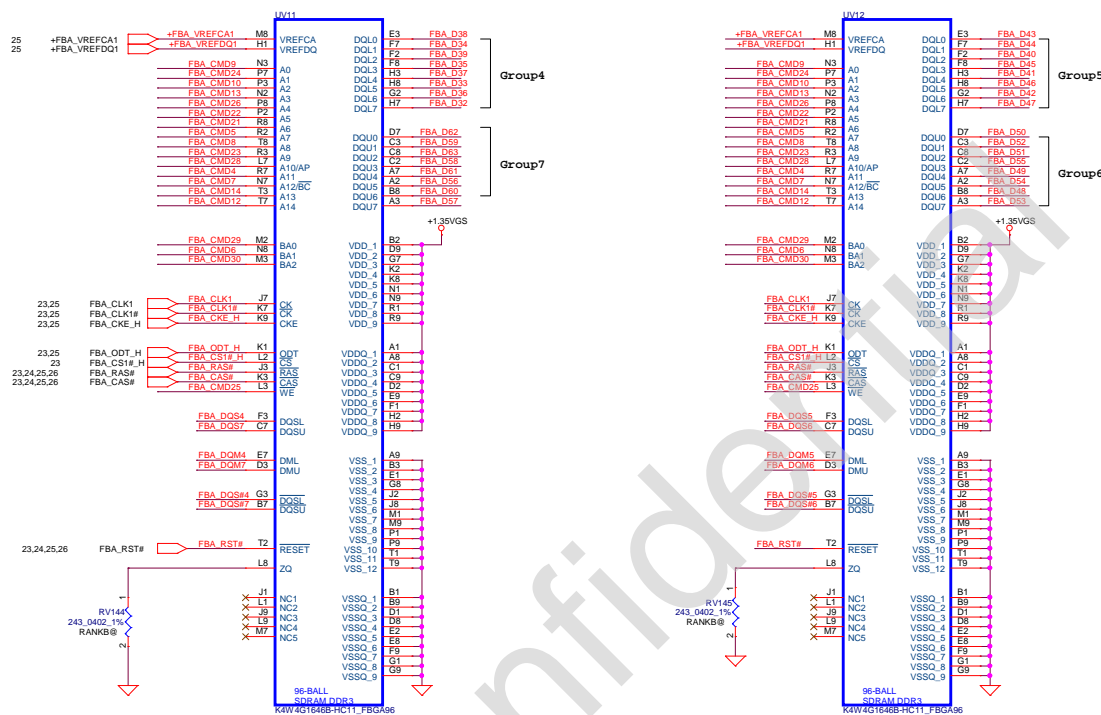
Address	Rank0	Rank1
FBX_CMD0	0..31	0..31
FBX_CMD1	32..63	32..63
FBX_CMD2	64..95	64..95
FBX_CMD3	96..127	96..127
FBX_CMD4	128..159	128..159
FBX_CMD5	160..191	160..191
FBX_CMD6	192..223	192..223
FBX_CMD7	224..255	224..255
FBX_CMD8	256..287	256..287
FBX_CMD9	288..319	288..319
FBX_CMD10	320..351	320..351
FBX_CMD11	352..383	352..383
FBX_CMD12	384..415	384..415
FBX_CMD13	416..447	416..447
FBX_CMD14	448..479	448..479
FBX_CMD15	480..511	480..511
FBX_CMD16	512..543	512..543
FBX_CMD17	544..575	544..575
FBX_CMD18	576..607	576..607
FBX_CMD19	608..639	608..639
FBX_CMD20	640..671	640..671
FBX_CMD21	672..703	672..703
FBX_CMD22	704..735	704..735
FBX_CMD23	736..767	736..767
FBX_CMD24	768..799	768..799
FBX_CMD25	800..831	800..831
FBX_CMD26	832..863	832..863
FBX_CMD27	864..895	864..895
FBX_CMD28	896..927	896..927
FBX_CMD29	928..959	928..959
FBX_CMD30	960..991	960..991

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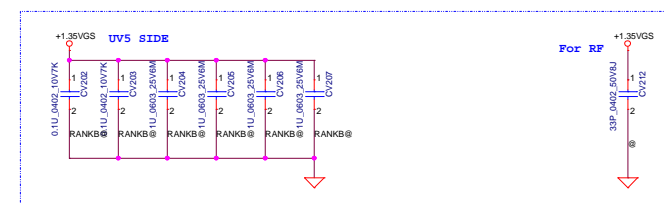
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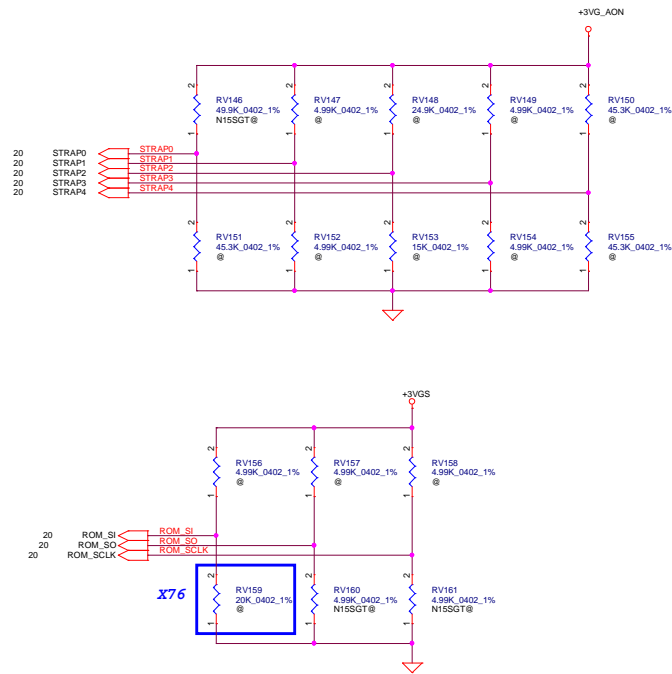
	Rank0		Rank1	
Address	0..31	32..63	0..31	32..63
Fbx_CMD0	ODT_L		ODT_L	
Fbx_CMD1			CS1#_L	
Fbx_CMD2	CS0#_L			
Fbx_CMD3	CKE_L		CKE_L	
Fbx_CMD4	A9	A9	A11	A11
Fbx_CMD5	A6	A6	A7	A7
Fbx_CMD6	A3	A3	BA1	BA1
Fbx_CMD7	A0	A0	A12	A12
Fbx_CMD8	A8	A8	A8	A8
Fbx_CMD9	A12	A12	A0	A0
Fbx_CMD10	A1	A1	A2	A2
Fbx_CMD11	RAS#	RAS#	RAS#	RAS#
Fbx_CMD12	A13	A13	A14	A14
Fbx_CMD13	BA1	BA1	A3	A3
Fbx_CMD14	A14	A14	A13	A13
Fbx_CMD15	CAS#	CAS#	CAS#	CAS#
Fbx_CMD16		ODT_H		ODT_H
Fbx_CMD17			CS1#_H	
Fbx_CMD18		CS0#_H		
Fbx_CMD19		CKE_H		CKE_H
Fbx_CMD20	RST	RST	RST	RST
Fbx_CMD21	A7	A7	A6	A6
Fbx_CMD22	A4	A4	A5	A5
Fbx_CMD23	A11	A11	A9	A9
Fbx_CMD24	A2	A2	A1	A1
Fbx_CMD25	A10	A10	WE#	WE#
Fbx_CMD26	A5	A5	A4	A4
Fbx_CMD27	BA2	BA2		
Fbx_CMD28	WE#	WE#	A10	A10
Fbx_CMD29	BA0	BA0	BA0	BA0
Fbx_CMD30			BA2	BA2





	Rank0		Rank1	
Address	0..31	32..63	0..31	32..63
FBX_CMD0	ODT_L		ODT_L	
FBX_CMD1			CSI#_L	
FBX_CMD2	CS0#_L			
FBX_CMD3	CKE_L		CKE_L	
FBX_CMD4	A9	A9	A11	A11
FBX_CMD5	A6	A6	A7	A7
FBX_CMD6	A3	A3	BA1	BA1
FBX_CMD7	A0	A0	A12	A12
FBX_CMD8	A8	A8	A8	A8
FBX_CMD9	A12	A12	A0	A0
FBX_CMD10	A1	A1	A2	A2
FBX_CMD11	RAS#	RAS#	RAS#	RAS#
FBX_CMD12	A13	A13	A14	A14
FBX_CMD13	BA1	BA1	A3	A3
FBX_CMD14	A14	A14	A13	A13
FBX_CMD15	CAS#	CAS#	CAS#	CAS#
FBX_CMD16		ODT_H		ODT_H
FBX_CMD17				CSI#_H
FBX_CMD18		CS0#_H		
FBX_CMD19		CKE_H		CKE_H
FBX_CMD20	RST	RST	RST	RST
FBX_CMD21	A7	A7	A6	A6
FBX_CMD22	A4	A4	A5	A5
FBX_CMD23	A11	A11	A9	A9
FBX_CMD24	A2	A2	A1	A1
FBX_CMD25	A10	A10	WE#	WE#
FBX_CMD26	A5	A5	A4	A4
FBX_CMD27	BA2	BA2		
FBX_CMD28	WE#	WE#	A10	A10
FBX_CMD29	BA0	BA0	BA0	BA0
FBX_CMD30			BA2	BA2





Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

X76

GPU	FB Memory (DDR3)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N15S-GT	Hynix 900MHz	H5TC4G63AFR-11C	0x3	PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff
	256M x 16	PD 20K	0x4						
	Micron 900MHz	MT41J256M16HA-093G:E	0x4						
	256M x 16	PD 24.9K	0x5						
	Samsung 900MHz	K4W4G1646D-BC1A	0x5						
	256M x 16	PD 30.1K							

VRAM	X76	VRAM P/N
Samsung	X76409JVL01	SA00005SH10
	X76409JVL51 (1G 32Mx16)	
Micron	X76409JVL02	SA00005M100
	X76409JVL02 (2G 64Mx32)	
Hynix		

GPU	FB Memory (DDR3)		STRAP3	STRAP2	STRAP1	STRAP0	STRAP4	ROM_SI	ROM_SO	ROM_SCLK
N15V-GM	H5TC4G63AFR-11C		PD 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K
	256M x 16	0x4								
	MT41J256M16HA-093G:E		PU 10K	PU 10K	PD 10K	PU 10K				
	256M x 16	0xD								

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C									
B									
A									
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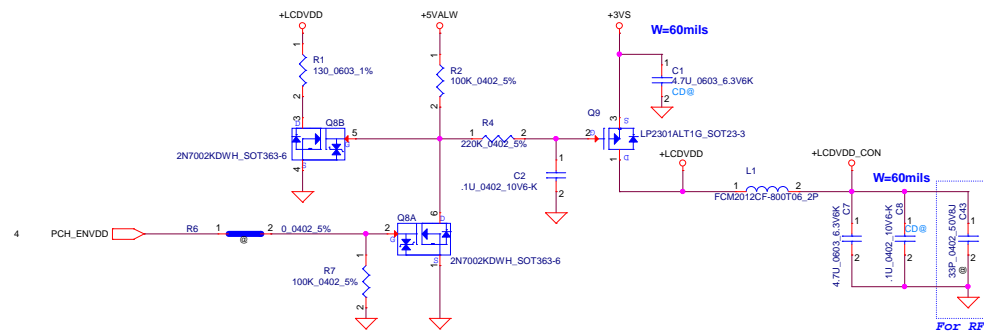
59

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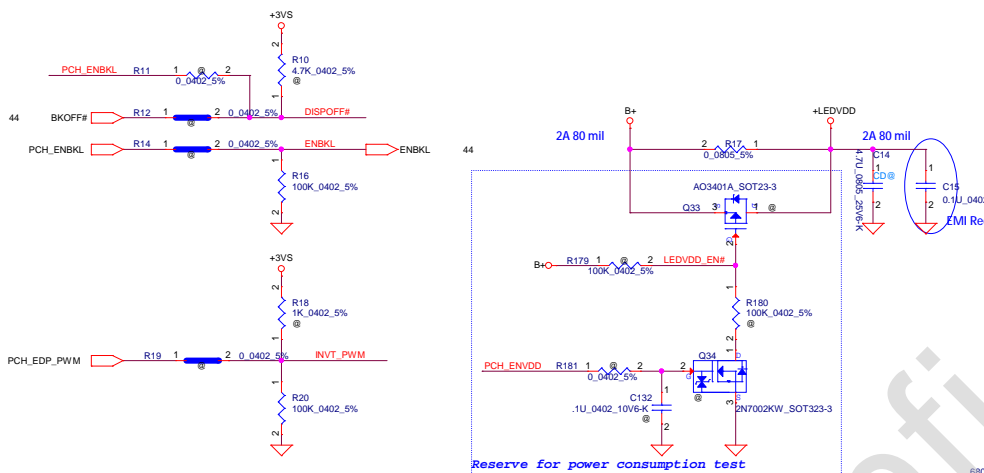
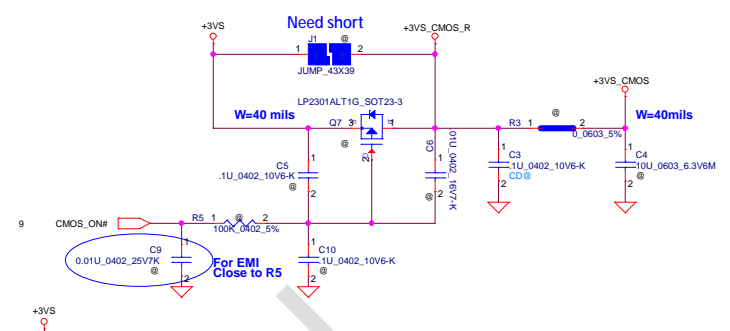
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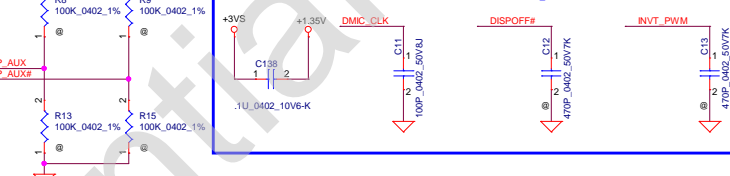
LCD POWER CIRCUIT



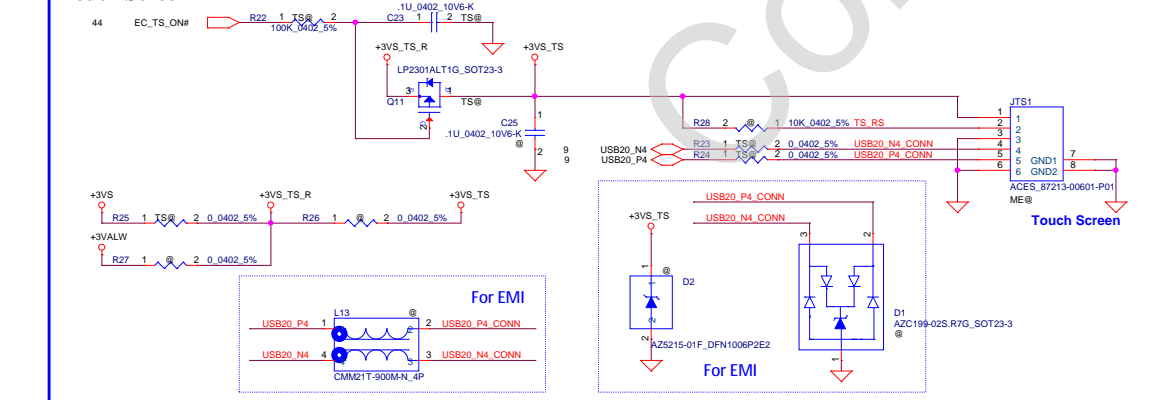
CMOS Camera



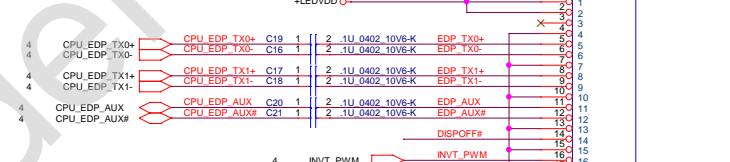
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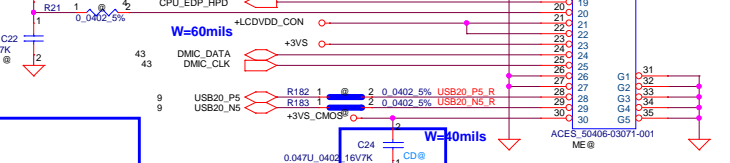
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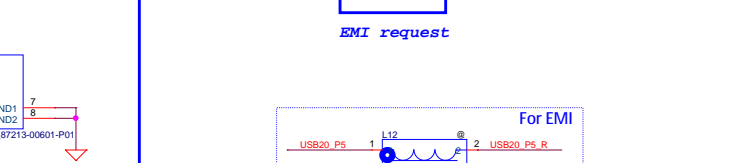
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EMI request



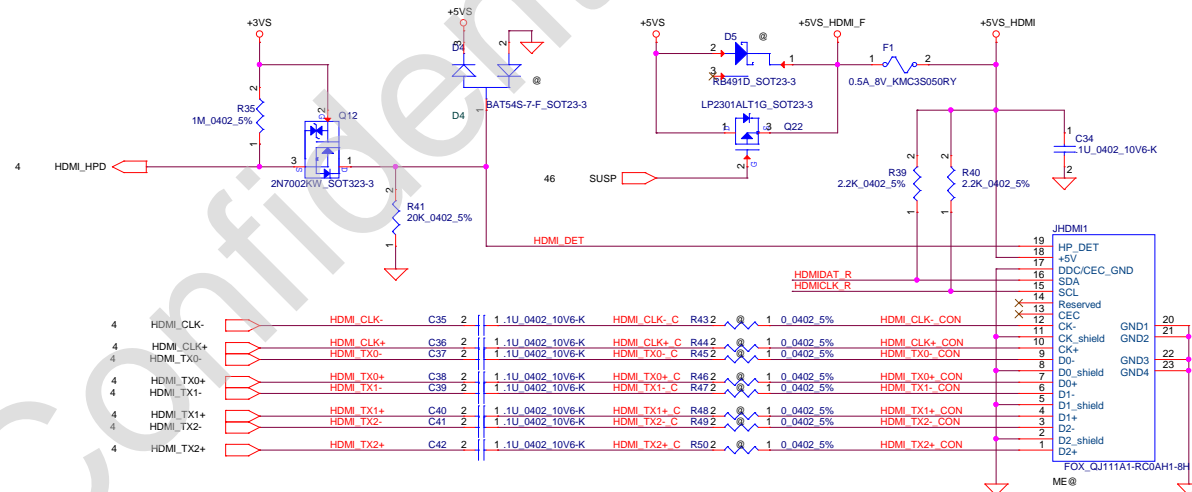
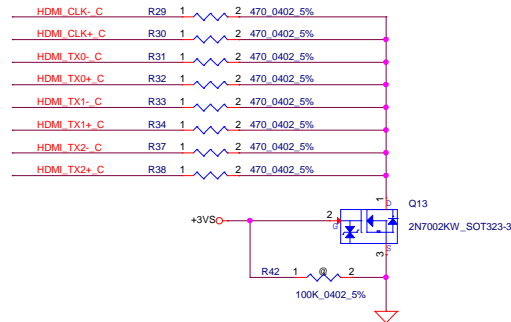
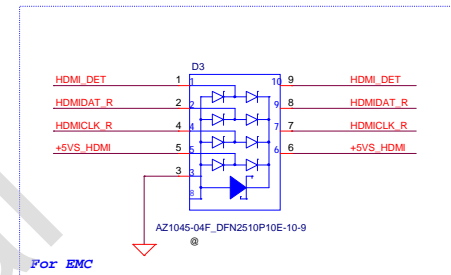
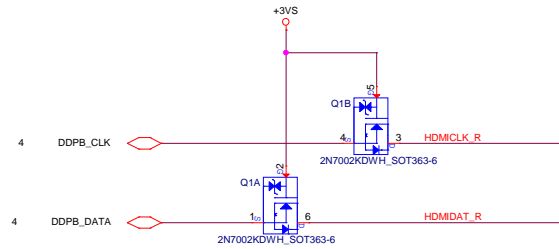
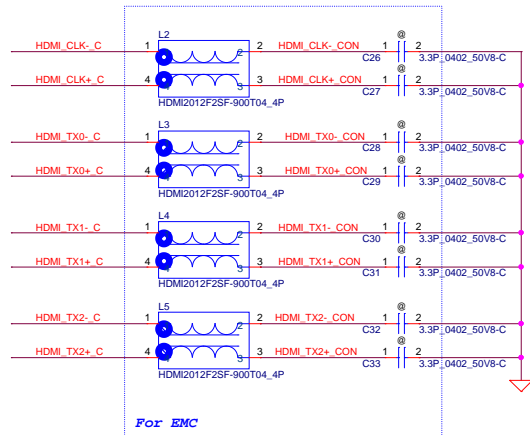
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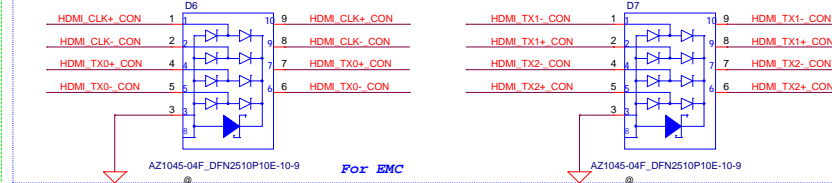
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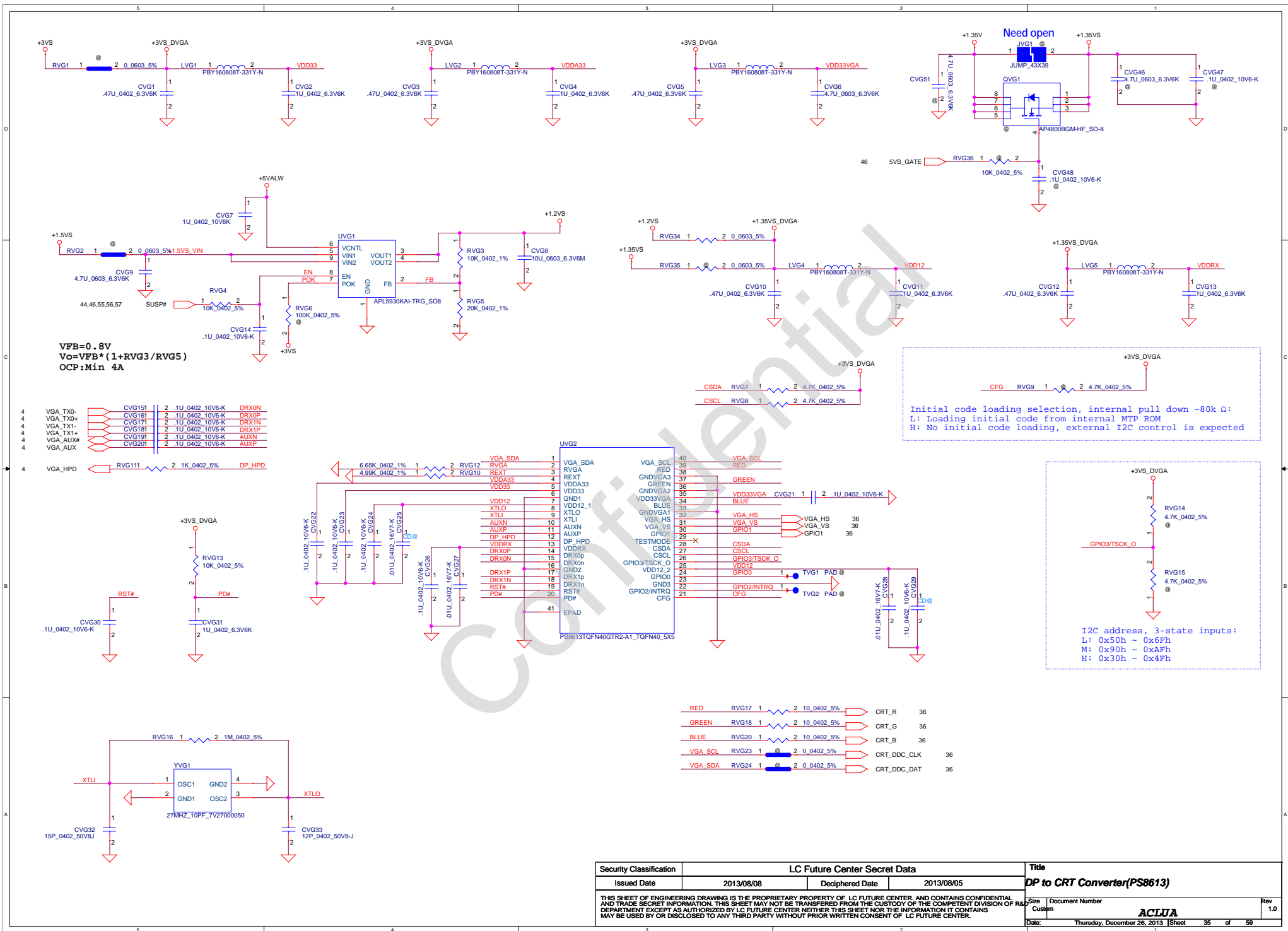
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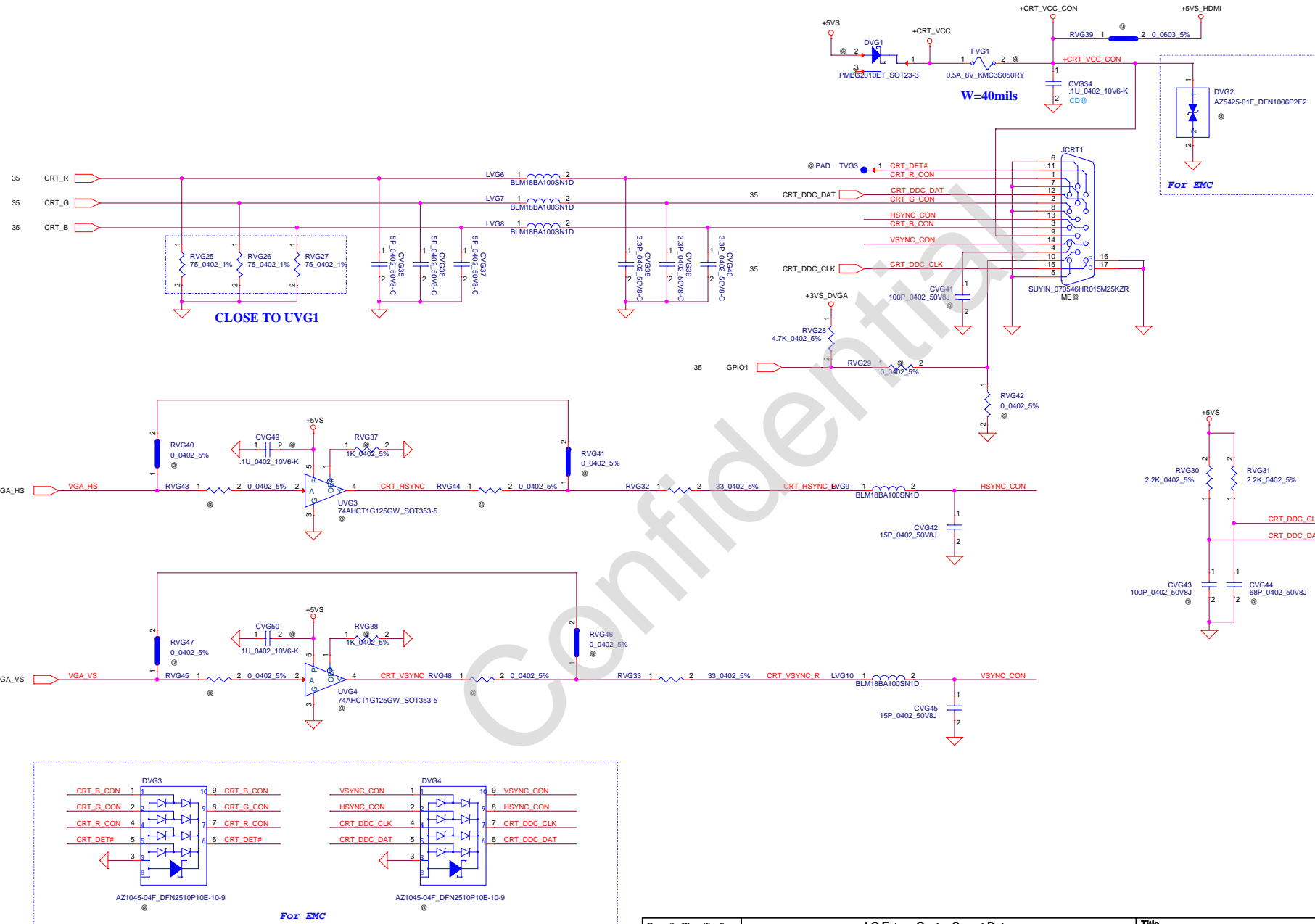
Close to JHDMI1



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CRT Connector



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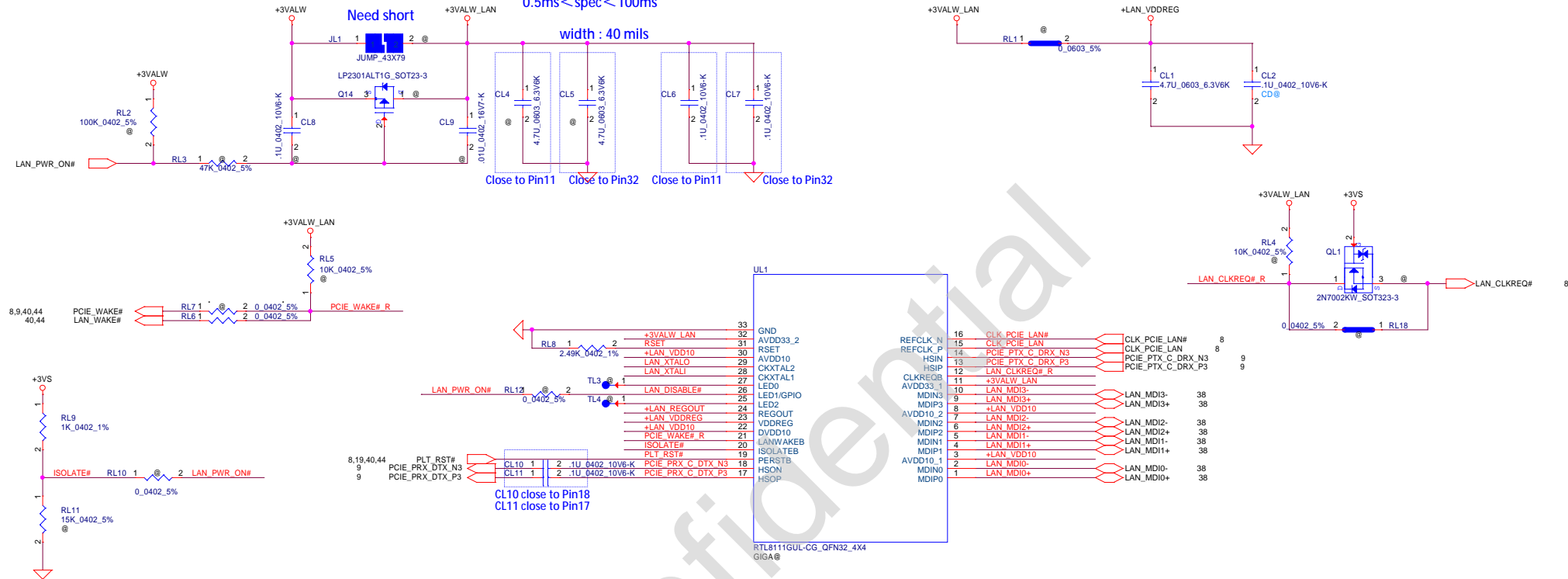
+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%):
0.5ms < spec < 100ms

Need short

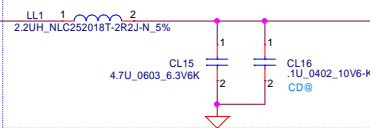
width : 40 mils

Close to Pin11 Close to Pin32 Close to Pin11 Close to Pin32



CL10 close to Pin18
CL11 close to Pin17

For RTL8111GUL/ RTL8106EUL (SWR mode)



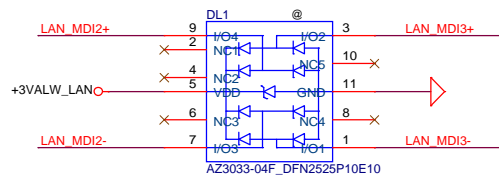
Layout Note: LL1 must be within 200mil to Pin36,
CL15, CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

Close to Pin3, 8, 22, 30

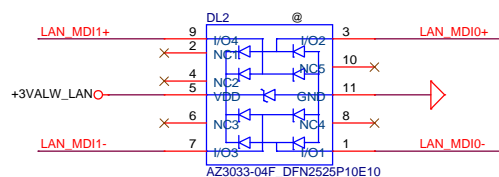
Close to Pin22(Reserved)

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				ACLU		

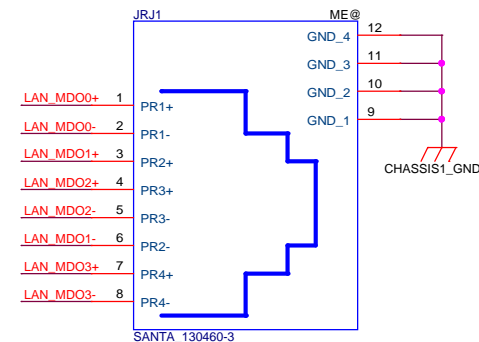
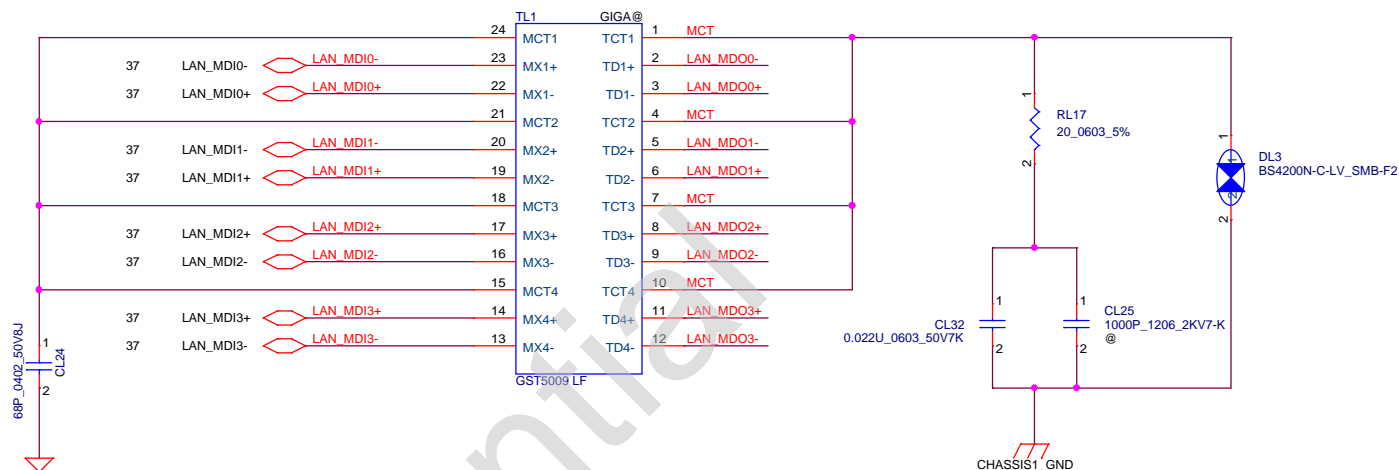
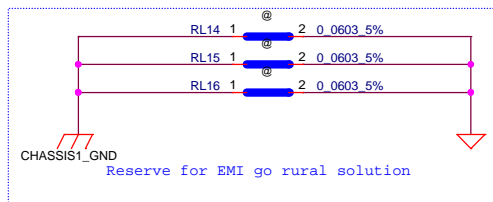
DL1/DL2
1'S PN:SC300003M00



Place Close to TL1

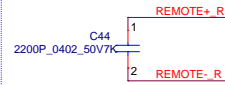


Place Close to TL2

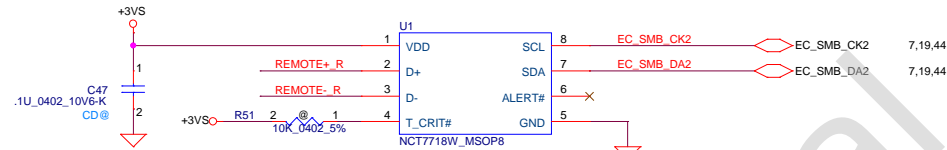


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Close to U1



SMSC thermal sensor placed near DIMM

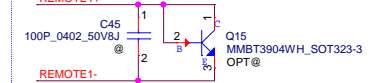


Address 1001_100xb

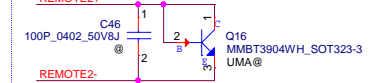


REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

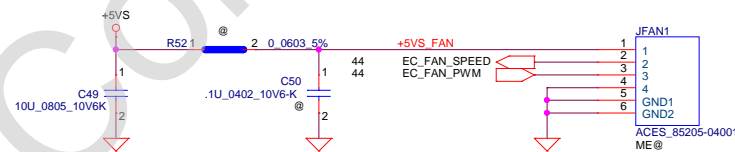
Near GPU&VRAM



Near CPU core

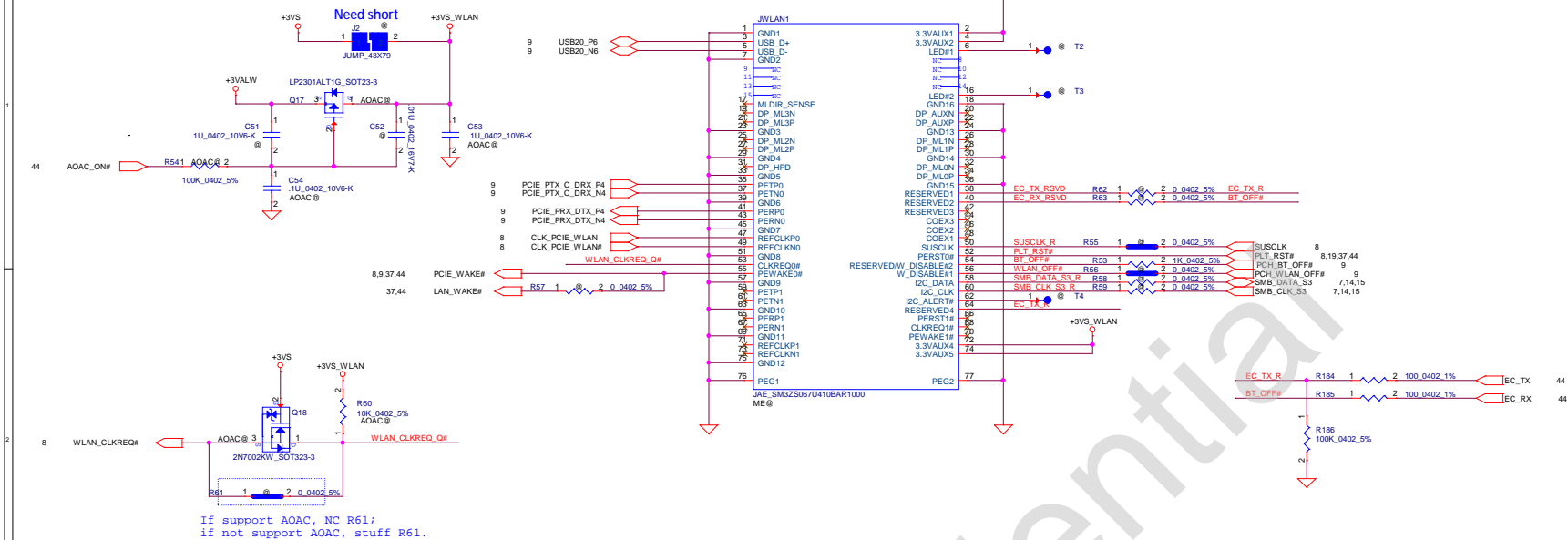


FAN Conn



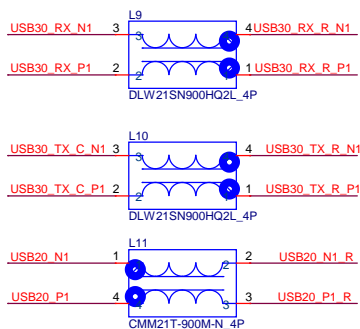
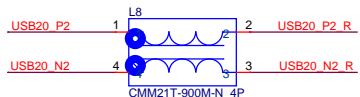
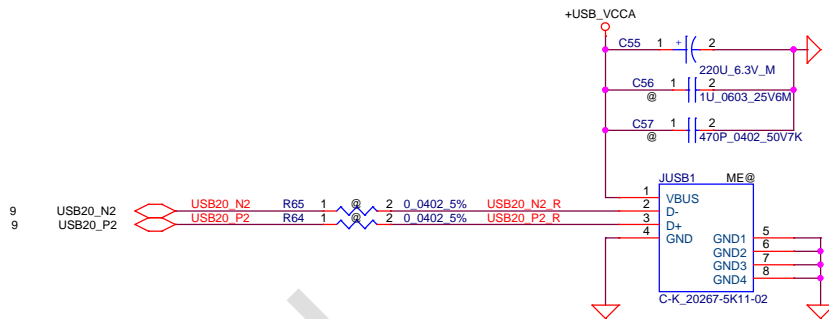
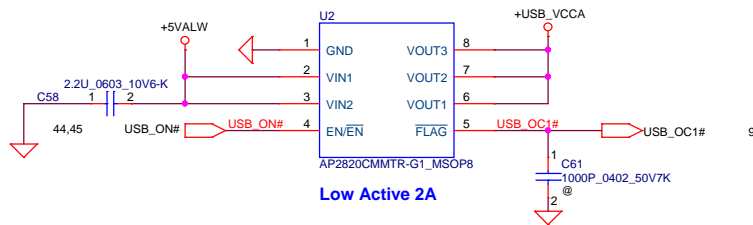
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Thermal sensor/FAN CONN	
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				Custom	1.0
				Date:	Thursday, December 26, 2013
				Sheet	39 of 59

Mini-Express Card(WLAN/WiMAX)

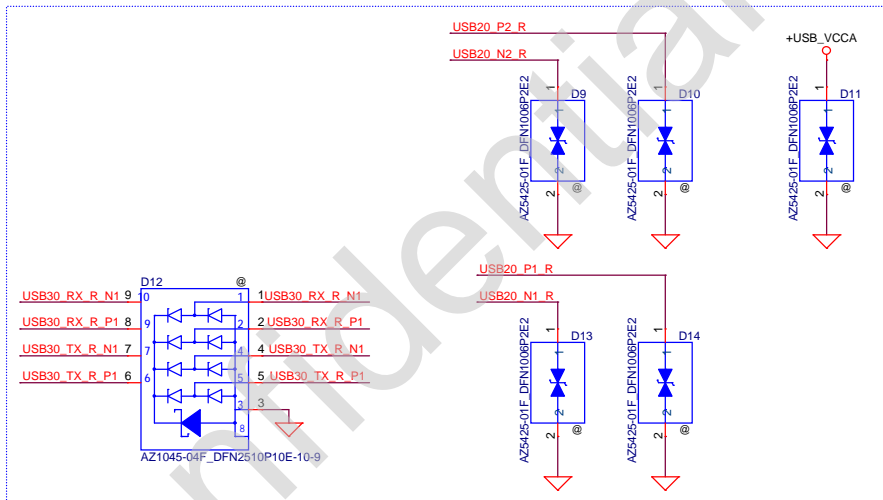


Security Classification	LC Future Center Secret Data			Title	
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Date: Thursday, December 26, 2013				Subject: AN of 60	

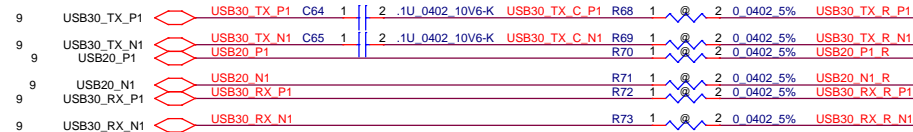
LEFT SIDE USB3.0 PORT X2



For EMC

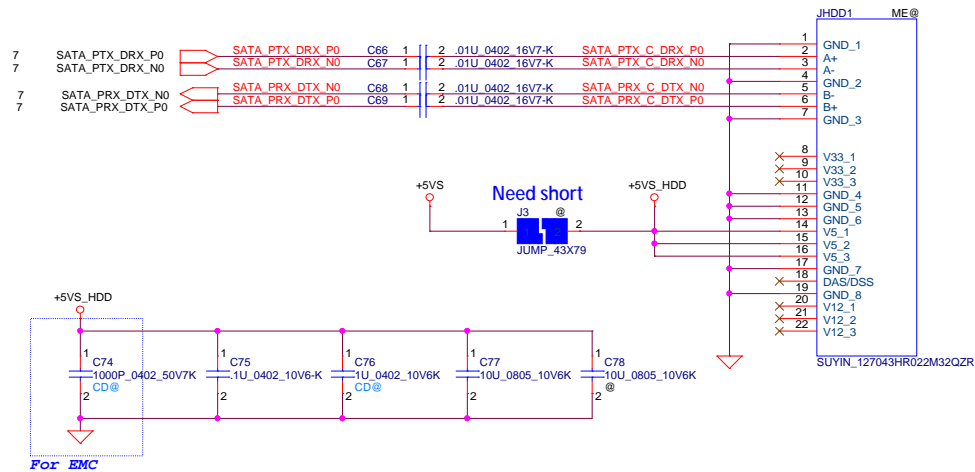


For EMC

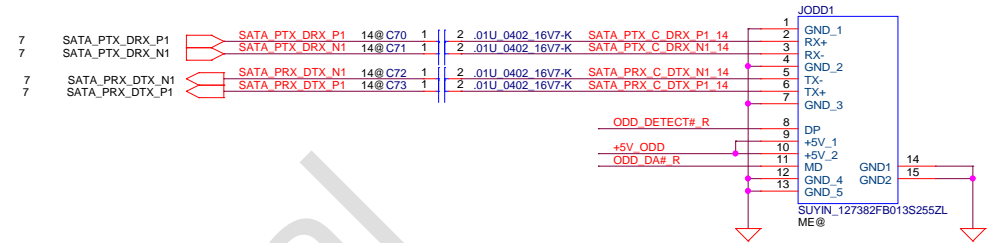


Security Classification				Title			
LC Future Center Secret Data				USB2.0/USB3.0 PORT (LEFT)			
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Size	Document Number	Rev	
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				Date:	Thursday, December 26, 2013	Sheet	41 of 59

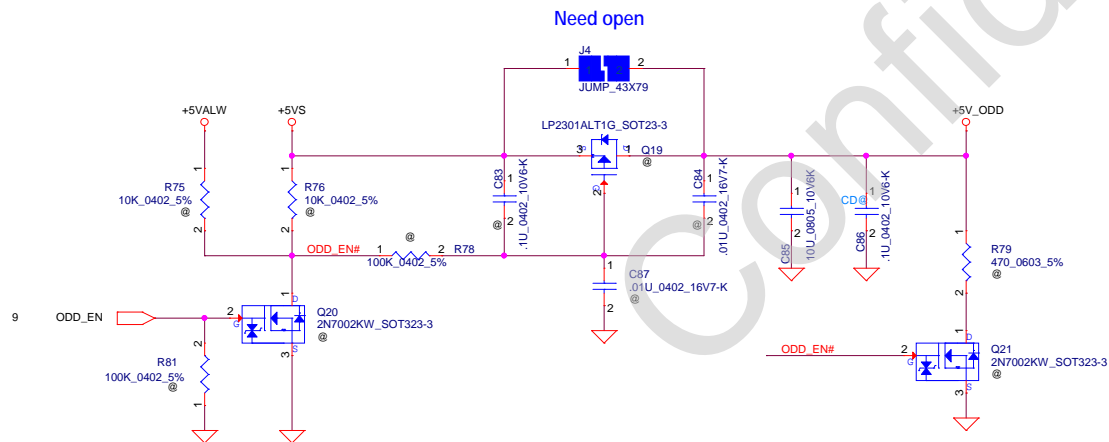
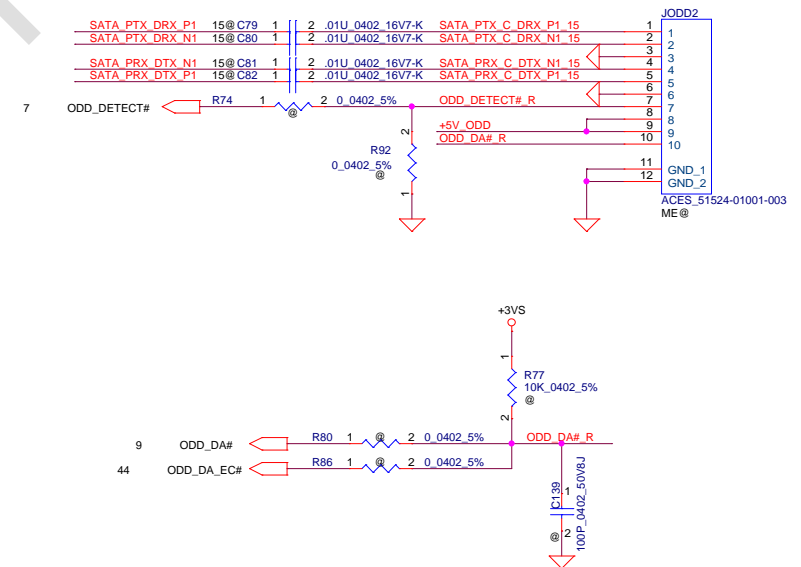
SATA HDD Conn.



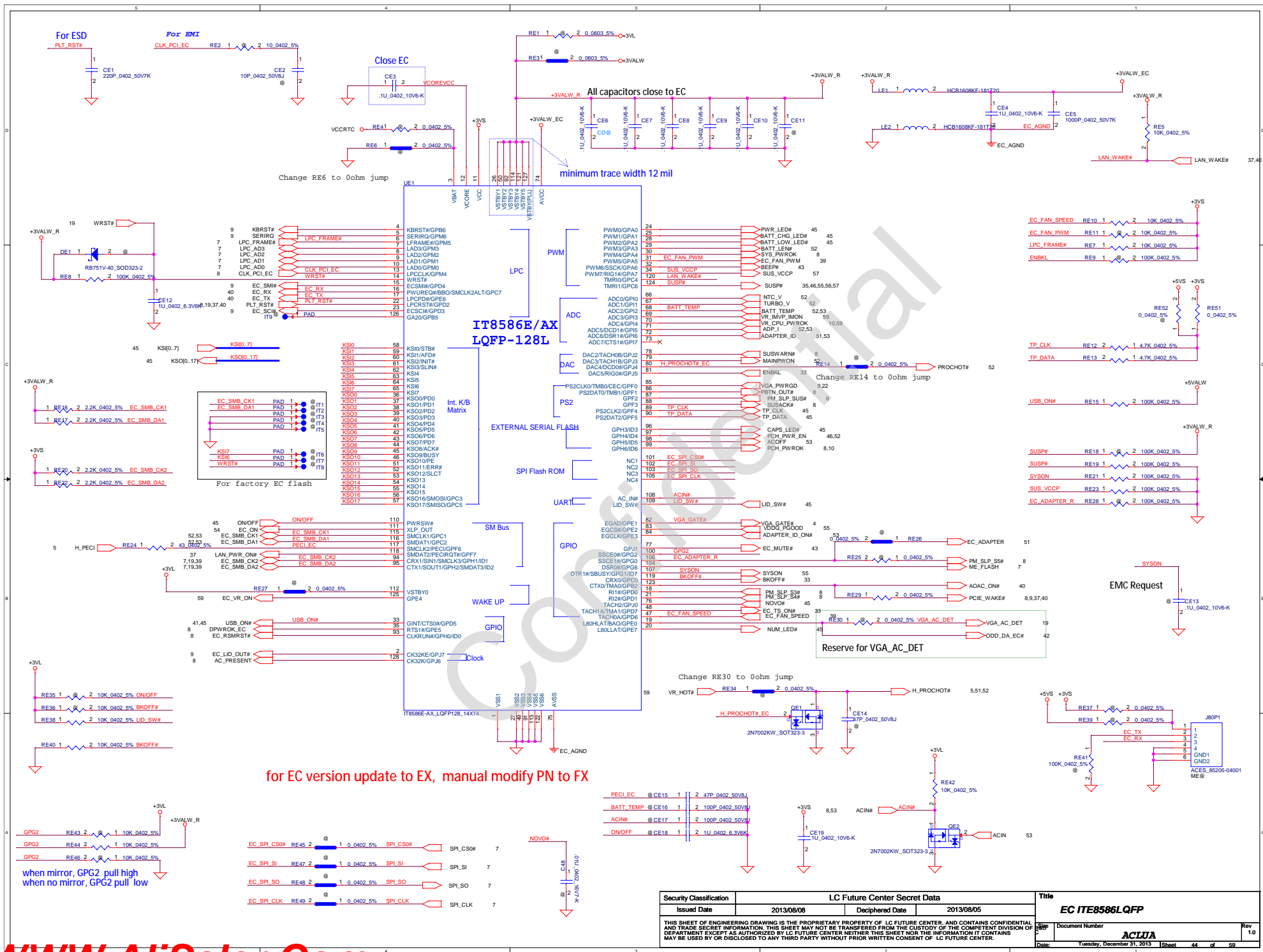
FOR 14" SATA ODD Conn.



FOR 15" SATA ODD FFC Conn

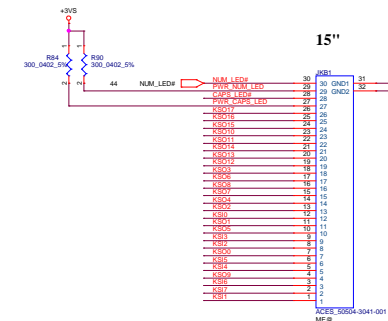
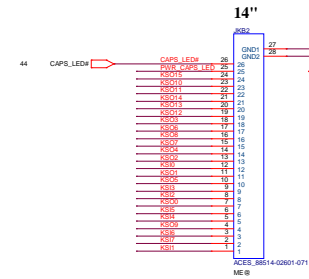
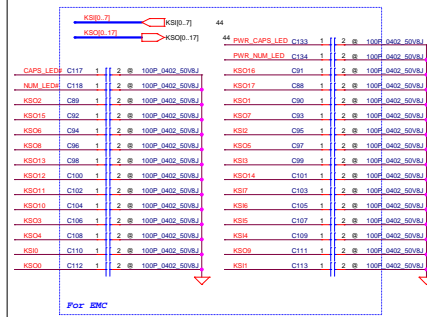


Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	HDD/ODD CONN	
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				Date: Thursday, December 26, 2013	Rev 1.0
				Sheet 42 of 59	

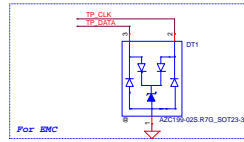
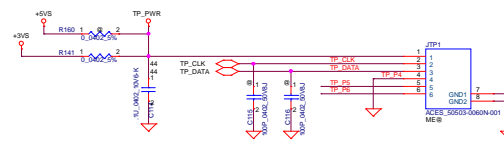


The schematic diagram illustrates the power supply circuit for the 68000 microprocessor. It features two input power pins, +3V/L and +3V/W, each connected to a network of resistors and a diode. The +3V/L pin is connected to a resistor R82 (100K_0402_5%) and a diode D15. The +3V/W pin is connected to a resistor R83 (100K_0402_5%) and a diode D15. The output of the circuit is labeled ONOFF and ONOFFSTRB. A ground symbol is shown at the bottom left.

K/B Connector

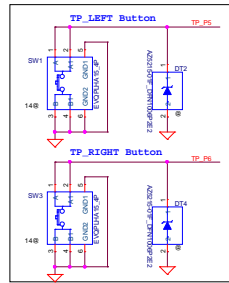


	14"	15"
FR_1_K211_14	K200_15	
FR_2_K317_14	K312_15	
FR_3_K316_14	K313_15	
FR_4_K309_14	K305_15	
FR_5_K314_14	K301_15	
FR_6_K315_14	K310_15	
FR_7_K300_14	K302_15	
FR_8_K312_14	K304_15	
FR_9_K313_14	K307_15	
FR_10_K305_14	K303_15	
FR_11_K301_14	K306_15	
FR_12_K310_14	K303_15	
FR_13_K302_14	K3012_15	
FR_14_K304_14	K3011_15	
FR_15_K307_14	K3014_15	
FR_16_K308_14	K3011_14	
FR_17_K306_14	K3010_15	
FR_18_K303_14	K3015_15	
FR_19_K302_14	K3016_15	
FR_20_K301_14	K3017_15	
FR_21_K3014_14	FR_LAD_PWR_15	
FR_22_K3011_14	CAPS_LADN_15	
FR_23_K3010_14	VDO_15	
FR_24_K3015_14	FRN_LADN_15	



1	VDD	1	VDD
2	CLK	2	CLK
3	DAT	3	DAT
4	GND	4	GND
5	TP-L	5	TP-L
6	TP-R	6	TP-R

1	VDD
2	CLK
3	DAT
4	GND
5	TP-L
6	TP-R

[illegible]

Right Side USB2.0 Port X 1 (USB/B)

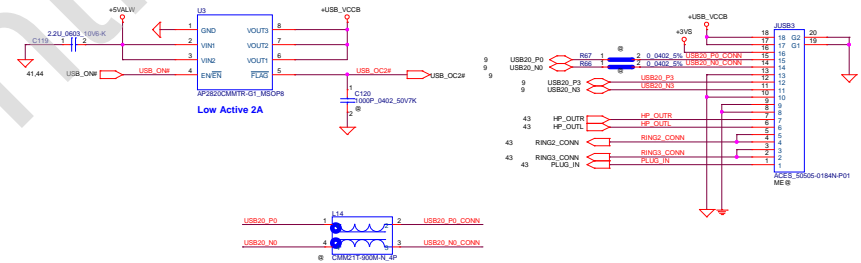
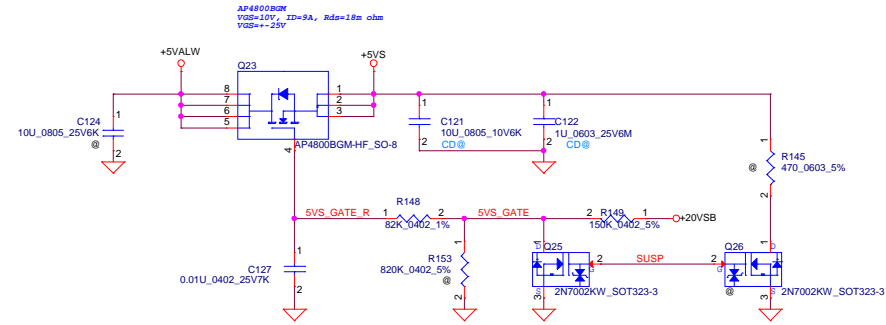


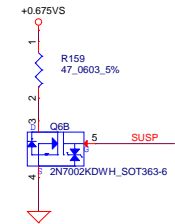
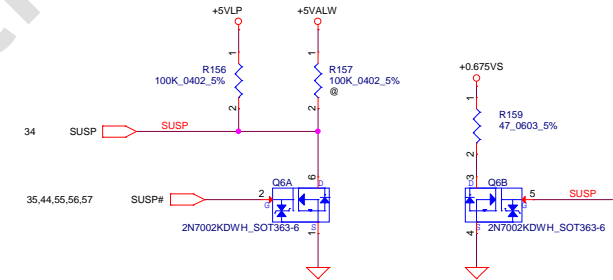
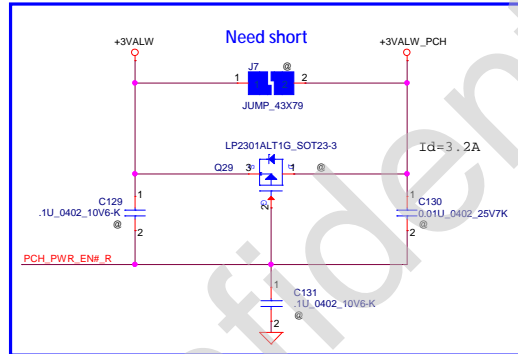
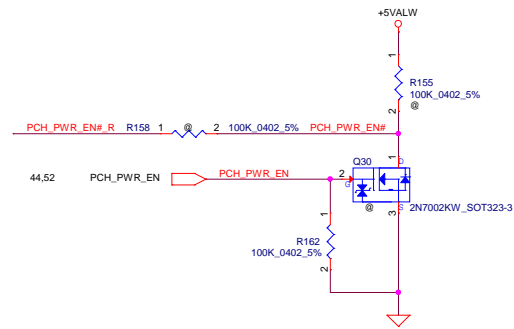
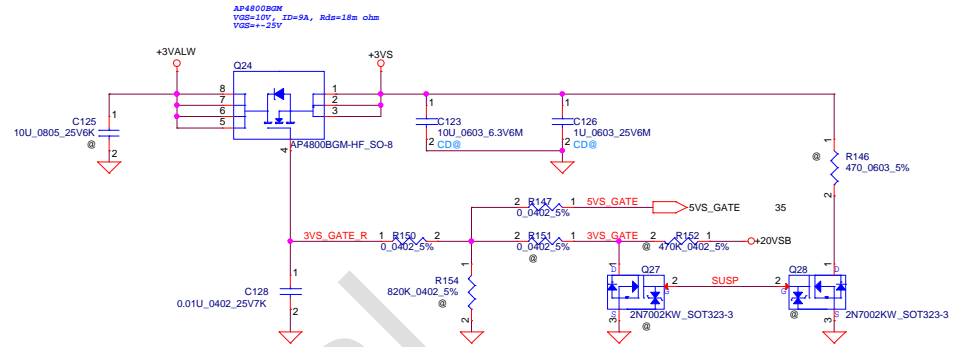
Figure 10 shows three LED driver circuit diagrams for the PWR_LED, BATT_LOW_LED, and BATT_CHG_LED. Each circuit includes a diode D19, a resistor R142 or R144, and a resistor R143 or R144. The PWR_LED circuit uses a 1K 0402 5% resistor. The BATT_LOW_LED circuit uses a 2K 0402 5% resistor. The BATT_CHG_LED circuit uses a 1K 0402 5% resistor. The LED is connected to the positive terminal of the battery.

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				2013/08/05	
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Rev		Doc Number		Rev	
1.0		ACUJA		1.0	
1		1		1	
2		2		2	
3		3		3	
4		4		4	
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100		100		100	

+5VALW to +5VS

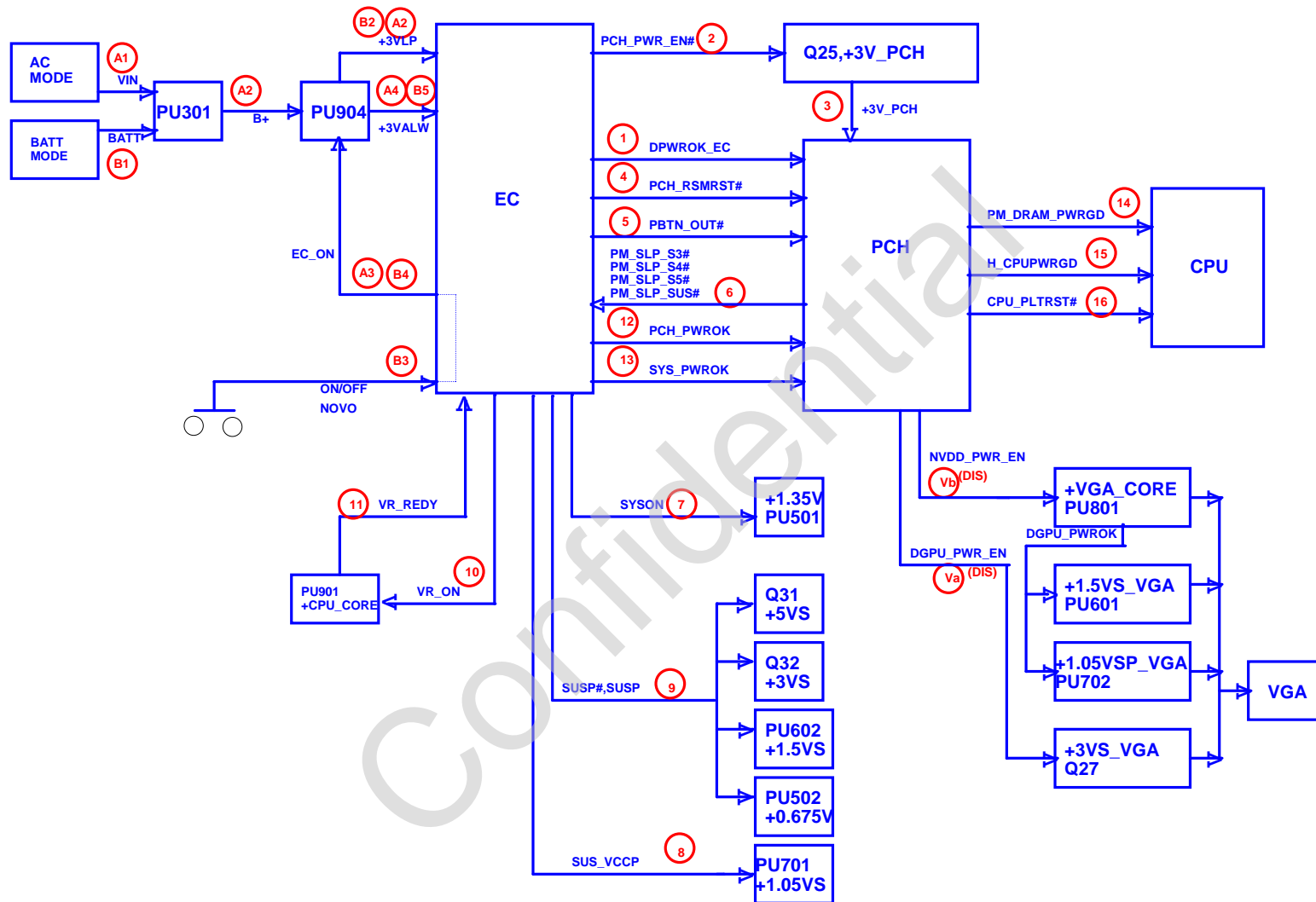


+3VALW to +3VS



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ACLUJA



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				Rev 1.0
				Date: Thursday, December 26, 2013 Sheet 47 of 59

LAN chip

UL1 100M@
RTL8106EUL-CG
SA000060C00

Transformer

TL1 100M@
TST1284A LF
SP050008C00

X76 BOM

ZZZ2 H4GXBT@
Hynix
X7603212001

ZZZ3 M4GXBT@
Micron
X7603212002

ZZZ4 H2GXBT@
Hynix
X7603212003

ZZZ5 H2GXBT@
Hynix
X7603212051

ZZZ6 M2GXBT@
Micron
X7603212052

ZZZ7 M2GXBT@
Micron
X7603212004

ZZZ8 S4GXBT@
Samsung
X7603212054

ZZZ9 S2GXBT@
Samsung
X7603212053

ZZZ10 14@
PCB PN
DA207Y00100

ZZZ11 15@
PCB PN
DA207Z00100

PCB_MB

UV1 N15VGM@
NV N15V-GM GPU
SA000064R00

RV155 N15VGM@
10K_0402_1%
SD03410028J

RV159 N15VGM@
10K_0402_1%
SD03410028J

RV160 N15VGM@
10K_0402_1%
SD03410028J

RV161 N15VGM@
10K_0402_1%
SD03410028J

Hynix 4G---256X16 *8 pcs X7603212001

UV5 H4T@
H5TC4G63AFR-11C
SA00005YL00

UV6 H4T@
H5TC4G63AFR-11C
SA00005YL00

UV7 H4T@
H5TC4G63AFR-11C
SA00005YL00

UV8 H4T@
H5TC4G63AFR-11C
SA00005YL00

RC100 H4T@
10K_0402_5%
SD02810028J

UV9 H4T@
H5TC4G63AFR-11C
SA00005YL00

UV10 H4T@
H5TC4G63AFR-11C
SA00005YL00

UV11 H4T@
H5TC4G63AFR-11C
SA00005YL00

UV12 H4T@
H5TC4G63AFR-11C
SA00005YL00

RV159 H4T@
20K_0402_1%
SD03420028J

Hynix 2G---256X16 *4 pcs X7603212051

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SA00005YL00

UV6 H2M@
H5TC4G63AFR-11C
SA00005YL00

UV7 H2M@
H5TC4G63AFR-11C
SA00005YL00

UV8 H2M@
H5TC4G63AFR-11C
SA00005YL00

RC107 H2M@
10K_0402_5%
SD02810028J

RV148 H2M@
10K_0402_1%
SD03410028J

RV151 H2M@
10K_0402_1%
SD03410028J

RV152 H2M@
10K_0402_1%
SD03410028J

RV154 H2M@
10K_0402_1%
SD03410028J

Micron 4G---256X16 *8 pcs X7603212002

UV5 M4T@
MT41J256M16HA-093G:E
SA00006010

UV6 M4T@
MT41J256M16HA-093G:E
SA00006010

UV7 M4T@
MT41J256M16HA-093G:E
SA00006010

UV8 M4T@
MT41J256M16HA-093G:E
SA00006010

RC100 M4T@
10K_0402_5%
SD02810028J

UV9 M4T@
MT41J256M16HA-093G:E
SA00006010

UV10 M4T@
MT41J256M16HA-093G:E
SA00006010

UV11 M4T@
MT41J256M16HA-093G:E
SA00006010

UV12 M4T@
MT41J256M16HA-093G:E
SA00006010

RV159 M4T@
24.9K_0402_1%
SD03420028J

Micron 2G---256X16 *4 pcs X7603212052

UV5 M2M@
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SA00006010

UV6 M2M@
MT41J256M16HA-093G:E
SA00006010

UV7 M2M@
MT41J256M16HA-093G:E
SA00006010

UV8 M2M@
MT41J256M16HA-093G:E
SA00006010

RC107 M2M@
10K_0402_5%
SD02810028J

RV148 M2M@
10K_0402_1%
SD03410028J

RV151 M2M@
10K_0402_1%
SD03410028J

RV152 M2M@
10K_0402_1%
SD03410028J

RV154 M2M@
10K_0402_1%
SD03410028J

Micron 2G---256X16 *4 pcs X7603212004

UV5 M2T@
MT41J256M16HA-093G:E
SA00006010

UV6 M2T@
MT41J256M16HA-093G:E
SA00006010

UV7 M2T@
MT41J256M16HA-093G:E
SA00006010

UV8 M2T@
MT41J256M16HA-093G:E
SA00006010

RC107 M2T@
10K_0402_5%
SD02810028J

RV159 M2T@
24.9K_0402_1%
SD03420028J

UV5 S4T@
K4W4G1646D-BC1A
SA000063F10

UV6 S4T@
K4W4G1646D-BC1A
SA000063F10

UV7 S4T@
K4W4G1646D-BC1A
SA000063F10

UV8 S4T@
K4W4G1646D-BC1A
SA000063F10

RC100 S4T@
10K_0402_5%
SD02810028J

UV9 S4T@
K4W4G1646D-BC1A
SA000063F10

UV10 S4T@
K4W4G1646D-BC1A
SA000063F10

UV11 S4T@
K4W4G1646D-BC1A
SA000063F10

UV12 S4T@
K4W4G1646D-BC1A
SA000063F10

RV159 S4T@
30.1K_0402_1%
SD03430128J

UV5 S2T@
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SA000063F10

UV6 S2T@
K4W4G1646D-BC1A
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UV7 S2T@
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SA000063F10

UV8 S2T@
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SA000063F10

RC107 S2T@
10K_0402_5%
SD02810028J

RV159 S2T@
30.1K_0402_1%
SD03430128J

PR9440 27K_0402_1%
N15VGM@

PR9434 7.5K_0402_1%
N15VGM@

PR9436 0.0402_5%
N15VGM@

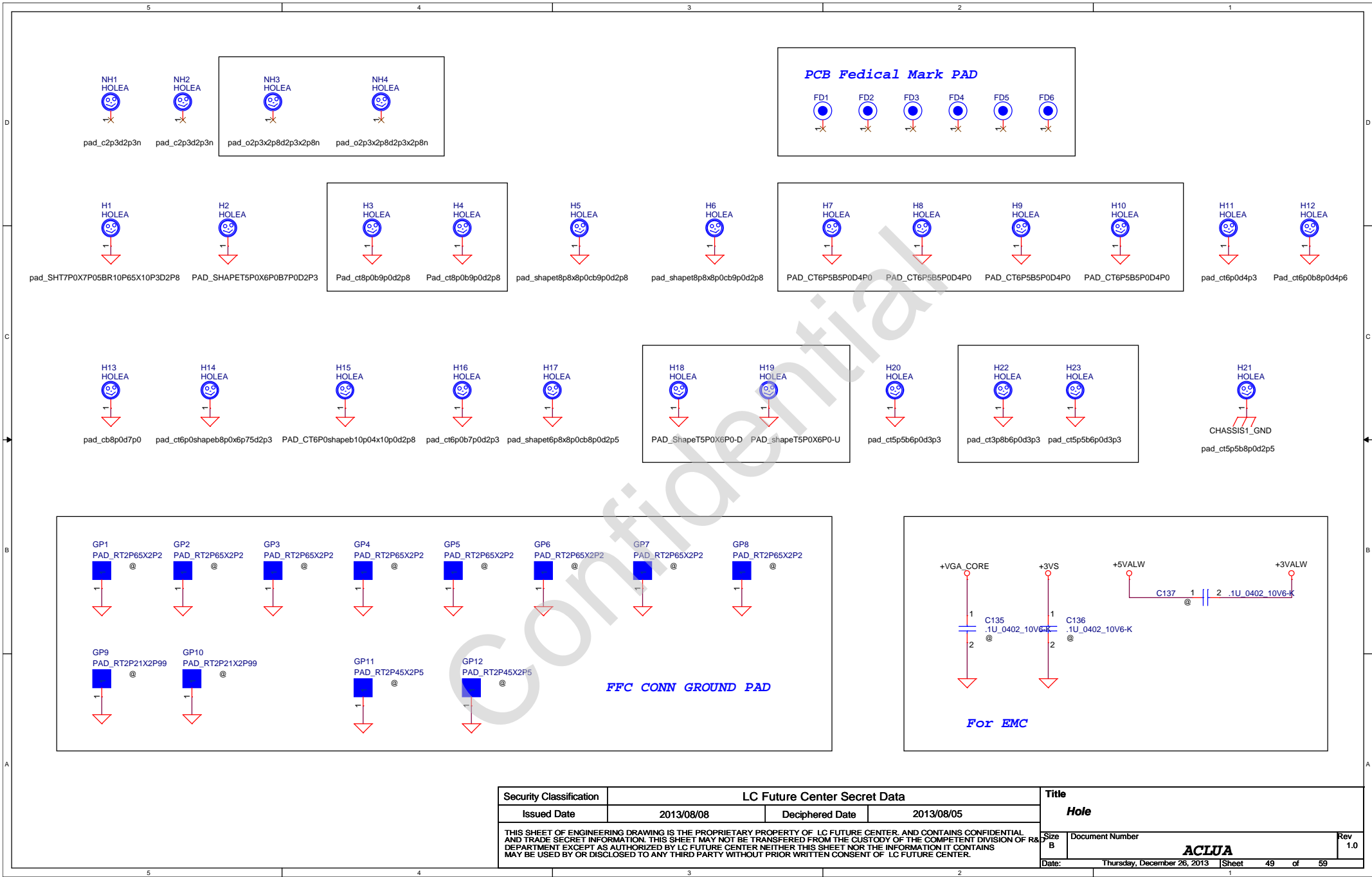
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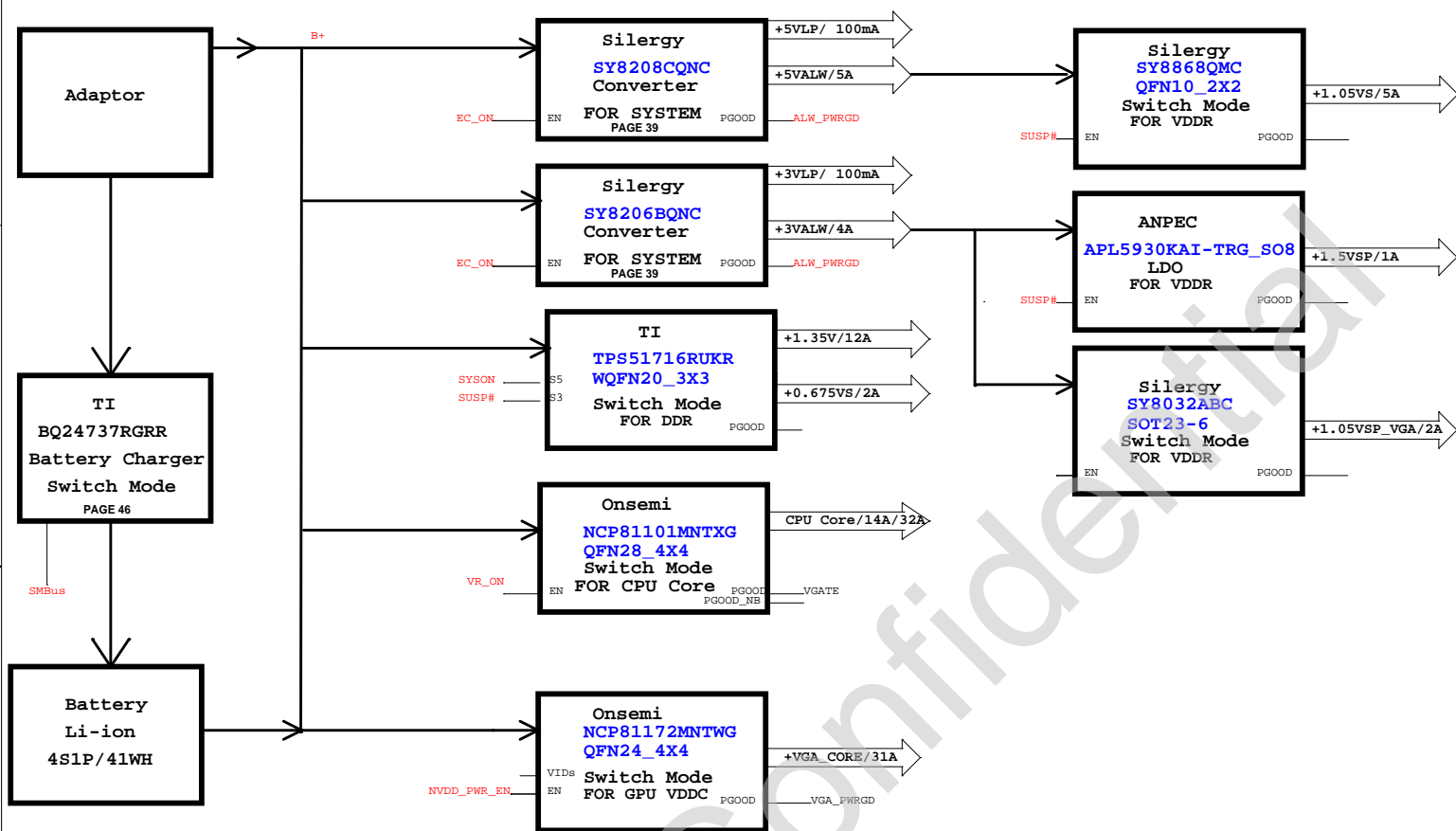
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PC1277 5600P_0402_25V7-K
N15VGM@

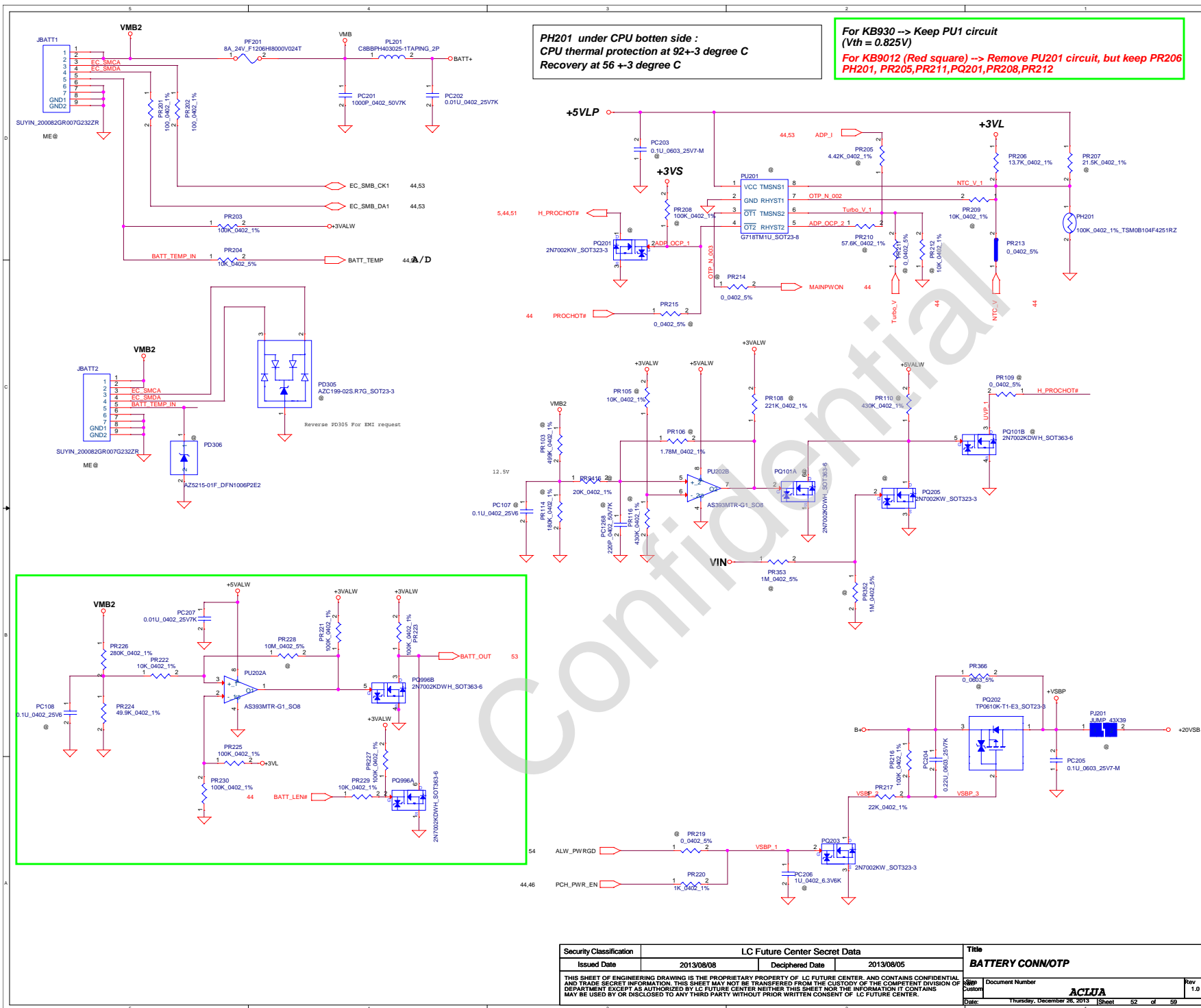
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Rev	Document Number	Virtual symbol	
C		ACLU	
Date	Wednesday, December 31, 2013	Sheet	48 of 59

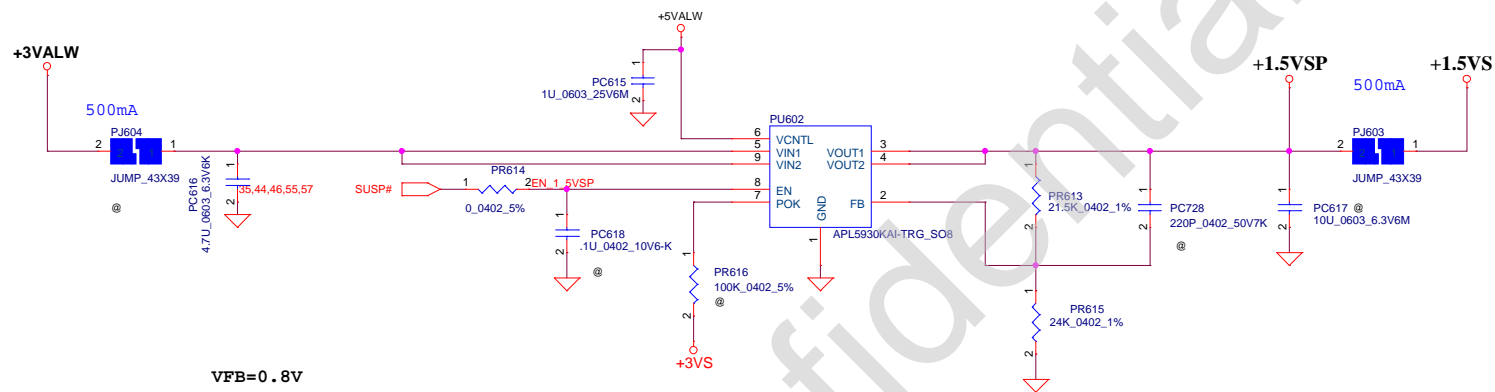
Rev 1.0



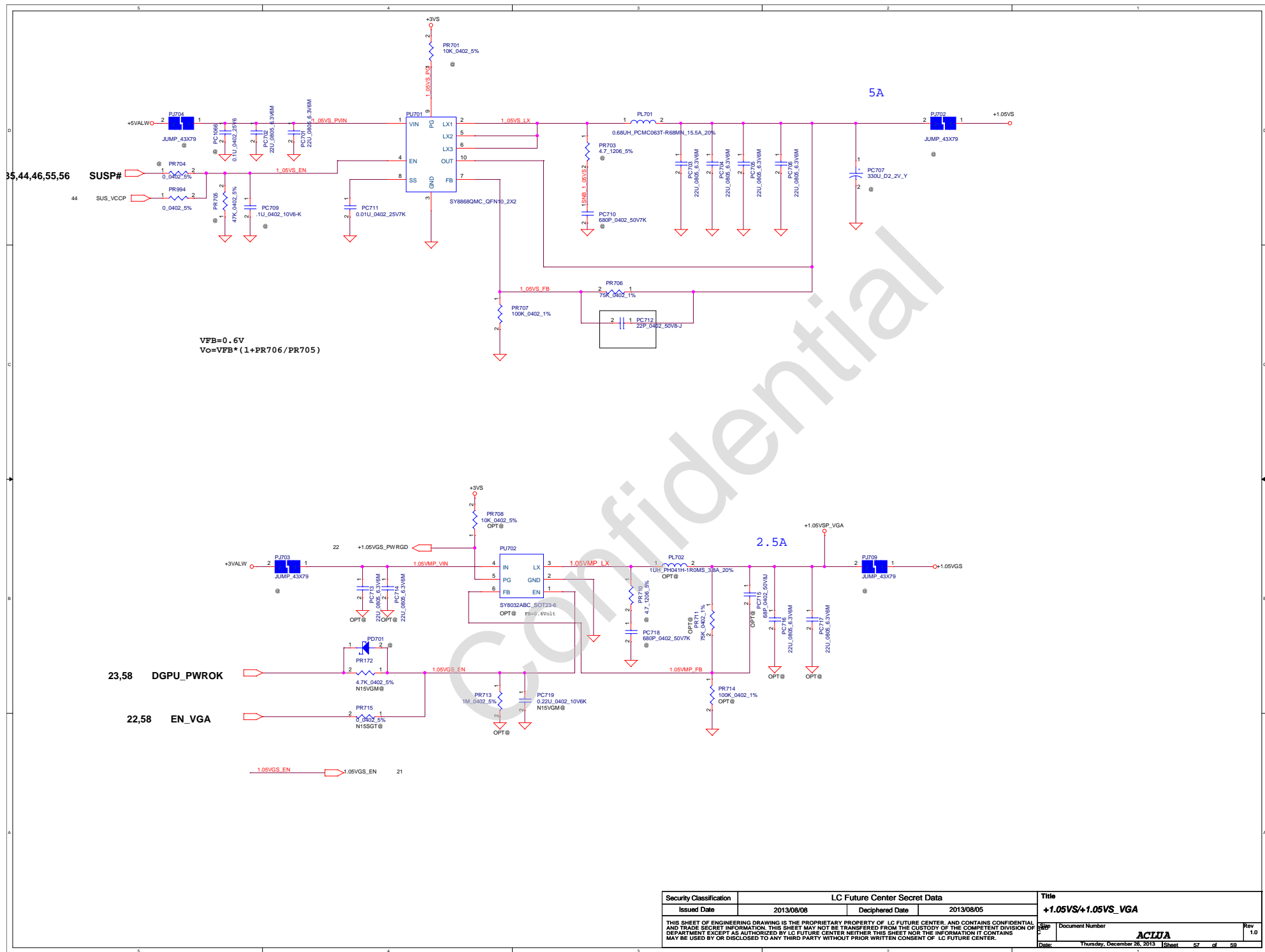


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